UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

REPORT NO. 106

FINAL REPORT - FLOW-GATING

by
Henry Guckel
Toshiro Kunihiro
Ronald K. Crow

March 24, 1961

This work was supported in part by the
Office of Naval Research under
Contract Nonr-1834(15).

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Summary

The following report concerns itself in principle with

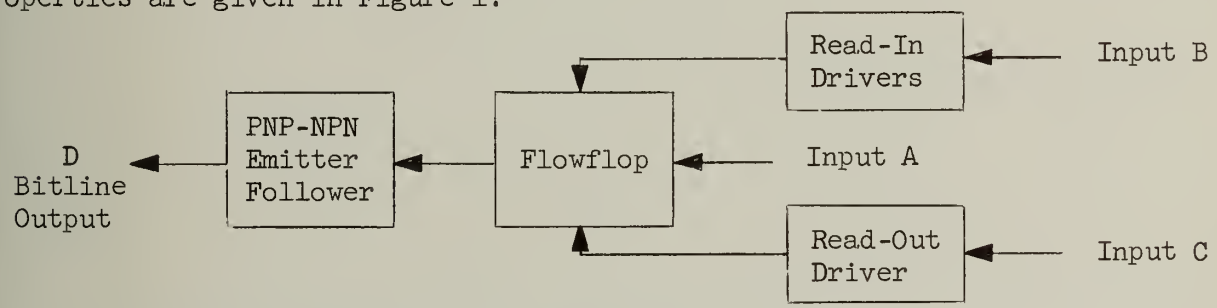
a) Transistor selection and evaluation
b) The basic design problem
c) The evaluation

of the flow-gating memory. The proposed mechanism was initially based upon Report No. 83 of this laboratory, but was modified to improve speed, reliability and driver-storage element balance.

The proposed system consists of

a) 14 flow-gating flipflops, which constitute a 1/4 word (3 transistors per bit)
b) The read-in driver (18/14 transistors per bit)
c) The read-out driver (10/14 transistors per bit)
d) Termination equipment (2/11 transistors per bit)

The system uses therefore five transistors per bit of which 12/14 are GF45011, 40/77 are N-101 and the remaining parts are of the N-100 type. The terminal properties are given in Figure 1.



	Voltage in Volts		Current in ma	
	One	Zero	One	Zero
A	$+\frac{3.2}{1.5}$	$-\frac{15}{1.5}$	$\frac{1.43}{0}$	$\frac{3.11}{2.67}$
B	$+\frac{3.2}{0.9}$	$-\frac{3.2}{0.9}$	0	$\frac{1.6}{0}$
C	$+\frac{3.2}{0.9}$	$-\frac{3.2}{0.9}$	0	$\frac{1.6}{0}$
D*	$\frac{2.86}{2.22}$	$\frac{2.63}{1.75}$	18	25

All table values are steady state values.

* The voltages given are at maximum allowable output currents. A voltage vs current output curve is contained in the report.

Figure 1

Flow-gating Memory Terminal Properties

In order to read out of the flowflop, C must be negative.
In order to read into the flowflop, B must be negative.
If not reading out, D is positive.

The AC behavior is discussed in considerable detail. The "read-in speed", after tolerance correction, is less than 90 nsec.; the read-out speed is in the vicinity of 80 nsec., when referenced to the input of the respective drivers. This apparently satisfies the proposed requirement of 150 nsec. access times.

Introduction

A storage system may in general be described by:

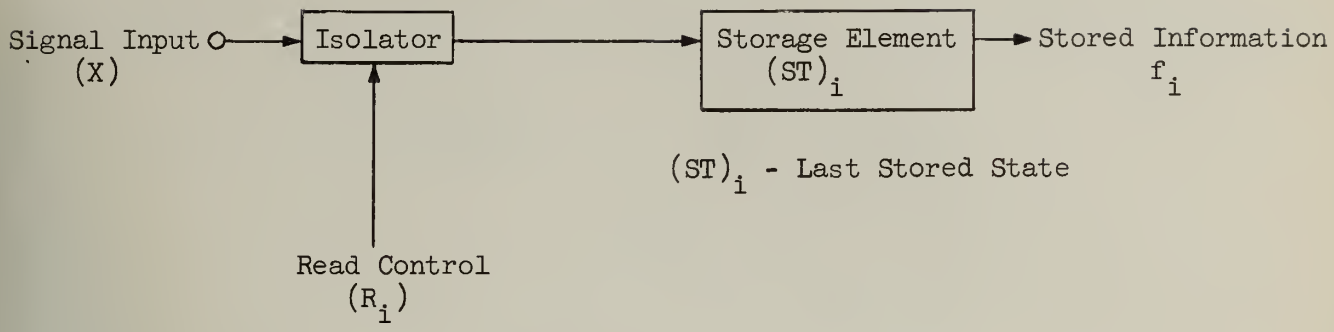


Figure 2

The output f_i is given by:

$$f_i = XR_i \vee ST_i\bar{R}_i \quad .$$

The use as a register system requires a gated output such that the final output is

$$Y = S_i(XR_i \vee ST_i\bar{R}_i)$$

where S_i is the send control. If $S_i = 0$ the output may be in either the one or zero band or floating.

A. Isolator

The isolator inhibits the flow of information to the storage element. It is in general not a simple AND or OR circuit unless a clearing and gating cycle is used. For a single-wire system, a double-gating method involves the following:

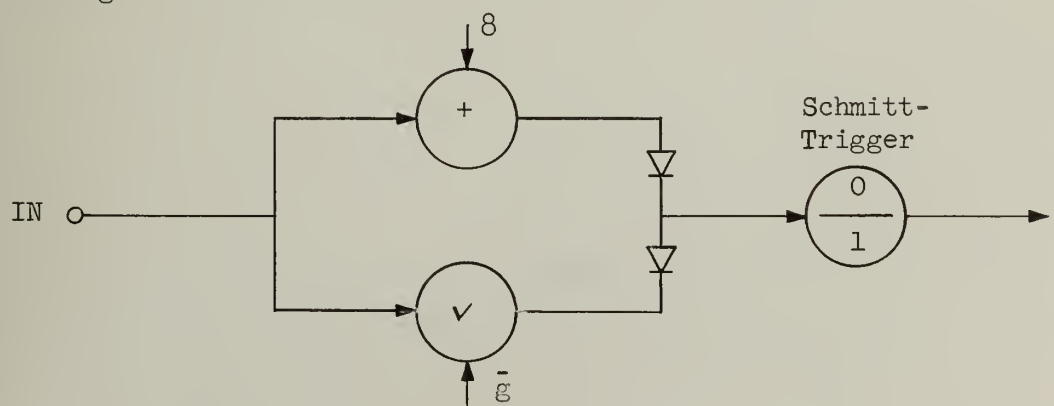
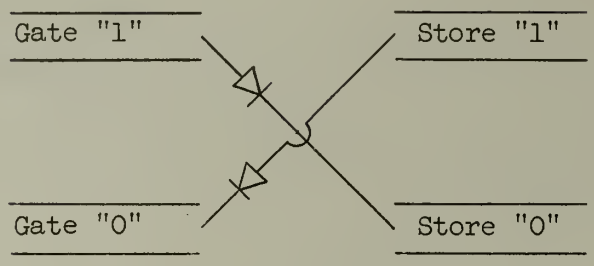


Figure 3

The complications are of course connected with the nature of the triggering point. The problem is evident from the following diagram:



$$Z_{Gate} < Z_{Store}$$

Figure 4

Two circuits are required for gating since the triggering point is in the feedback path, i.e. it has the potential of the last state. This in turn implies that a gating system which involves minimum complexity should have a trigger point isolated from feedback circuitry. A possible answer would be the following circuits:

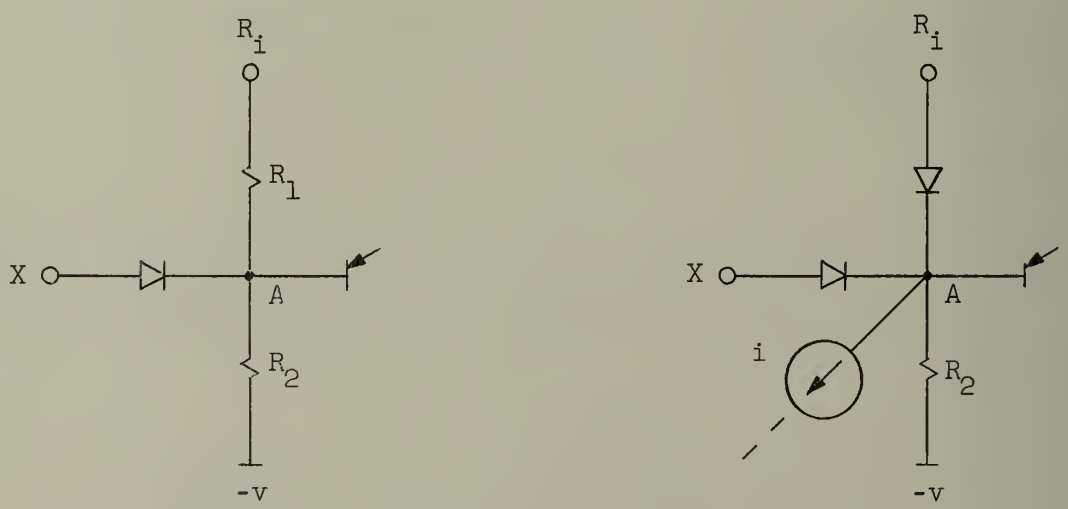


Figure 5

Direct gating is achieved by changing the potential of the divider. Either an analog (Figure 5a) or digital (Figure 5b) method may be used, with appropriate speed advantages for the latter method. The use of a constant current sink offers good pulse response. The logical output A occurs at $t_0 + \Delta_R$, where Δ_R is the inherent delay of the read driver.

$$A = XR_i \ [t_0 + \Delta_R]$$

B. Storage Element

The choice of the storage element is restricted by

a) Gate-method
b) Single-wire system requirement
c) Maximum allowable setting speed

The restrictions force the topology of an assymmetric flipflop. Since speed is essential a feedback path which does not involve collector delays is desired.

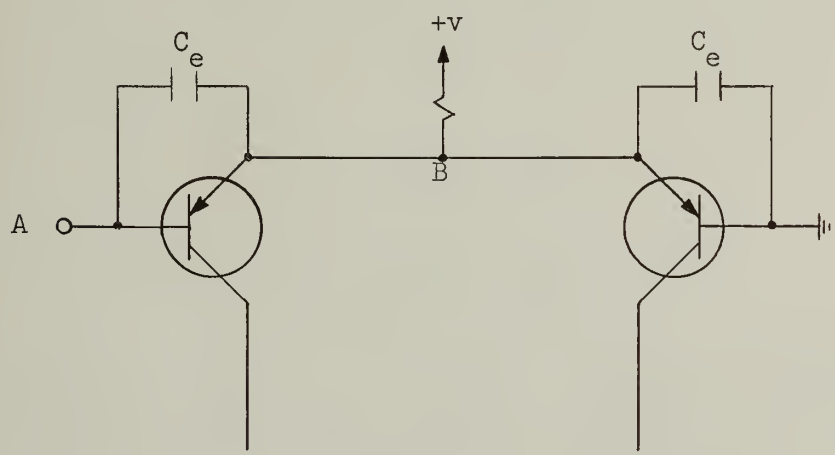


Figure 6

The topology is simply a difference amplifier. The output occurs at B:

$$B = A[\Delta_B] \vee ST_i$$

$$B = XR_i[t_0 + \Delta_R + \Delta_B] \vee ST_i \quad .$$

The timing relations are shown in the following figure:

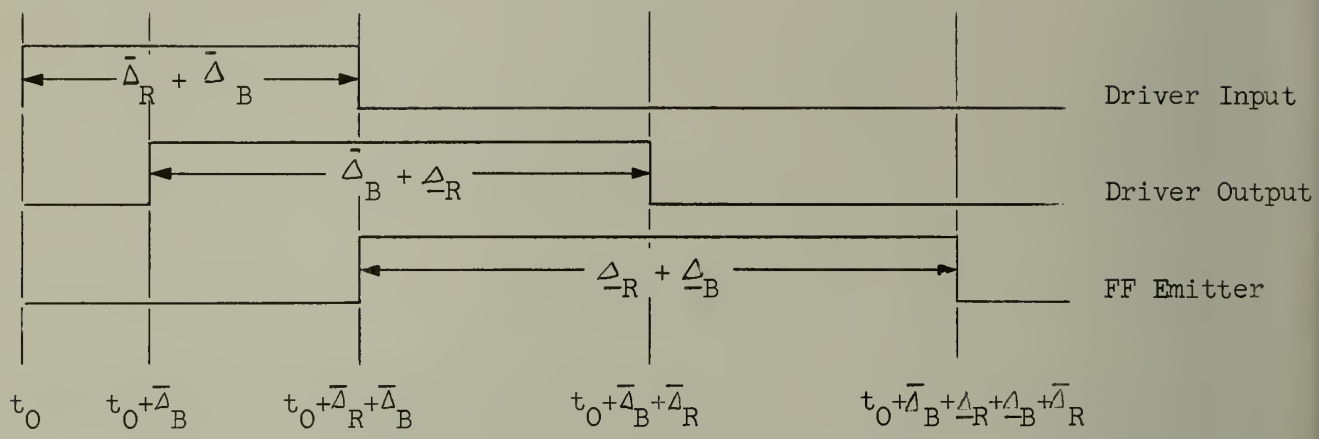


Figure 7

This method of gating provides considerable overlap between timing pulses. It allows large deviations of the Δ_i's from their average value. On this basis the safe driver-input pulse length may be defined as:

$$L_R = \overline{\Delta}_R + \overline{\Delta}_B + \Gamma$$

$$\Gamma = \text{Safety Factor}$$

$$\Gamma_{Min} = \overline{\Delta}_{R_{Max}} - \overline{\Delta}_{R_{Min}} + \overline{\Delta}_{B_{Max}} - \overline{\Delta}_{B_{Min}} \quad .$$

It should be noted that Δ_B may be different for a zero or one gating cycle. In any case, the worst deviation should be used. Since the information occurs at the emitter some time before $t = t_0 + L_R$ the quantity L_R may be used to define the access time. The obvious, but nevertheless important, point concerns the relation between driver and flipflop speed. For a fast system, both Δ_R and Δ_B are small; for a balanced system Δ_R and Δ_B are of the

same magnitude. Large differences indicate miss-match between driver and storage element design, and therefore an uneconomical and perhaps a misdesigned system. The minimum read pulse length is $(\Delta_B)_{Max}$. Hence the read-in time is given by:

$$(\Delta_B)_{Max} \leq t_{IN} < \overline{\Delta}_R + \overline{\Delta}_B + \Gamma \quad .$$

So far nothing has been said about the storing capability of the circuit. Information travel has been restricted to the emitter circuit. Suppose the gating circuit is ignored for the present and only the storing mechanism is considered.

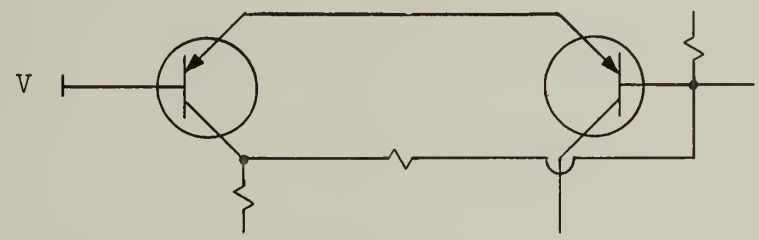


Figure 8

The desired topology is shown. The steady state store is of course obtained when the loop gain is larger than unity; the bistable behavior by proper biasing. The circuit is a Schmitt-Trigger with the input point on the left base. In order to change the gated circuit to this storing configuration the following circuit may be used:

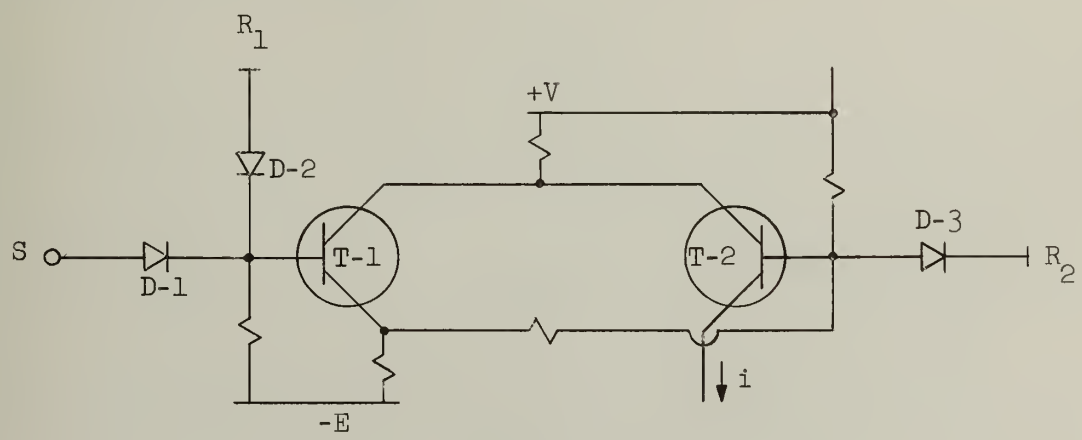


Figure 9

The function of the diodes has in part been discussed earlier. Their behavior is summarized as follows:

D-1	On During Gating
D-2	On During Store
D-3	On During Gating

R_1 and R_2 are the read signals. They are in time phase, but may differ in potential. The state of the flipflop may be sensed by considering the occurrence of current i. It is to be noted that the collector of T-2 may be considered as an isolated point.

Some comments may be made concerning the behavior during the transition period. In order to explain the mechanism of state retention, some of the properties of transistors are recalled.

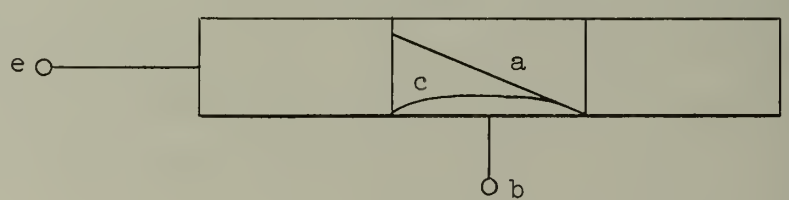


Figure 10

The minority carrier charge distribution in the transistor during conduction is given by curve a. During equilibrium conditions, i.e. the "off" condition the distribution is as shown by curve c. In order to turn the transistor off electron injection must occur at the base. This takes a finite amount of time (stored charge theories). The equivalent circuit yields similar results.

The initial voltage across the diffusion capacitance C_e is given by:

$$r_e i_e \approx \frac{kT}{q} \quad .$$

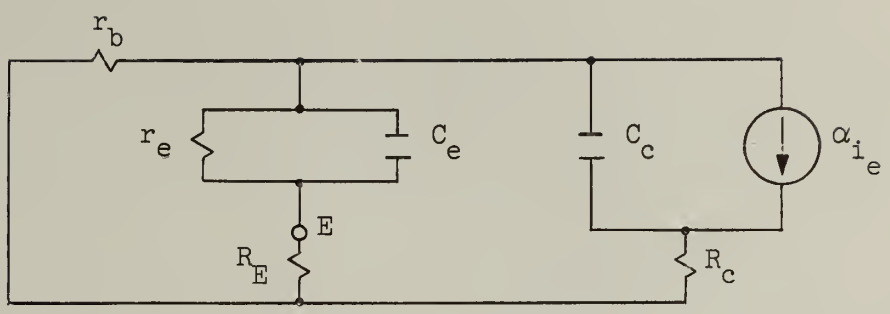


Figure 11

If the current is interrupted, the diffusion network remains active due to this stored charge.

As far as collector response is concerned, two questions must be answered:

1. Does the emitter-base diode become reverse biased during transitions?

2. If so, does this mean a loss of state?

The first question is answered by considering the following figure:

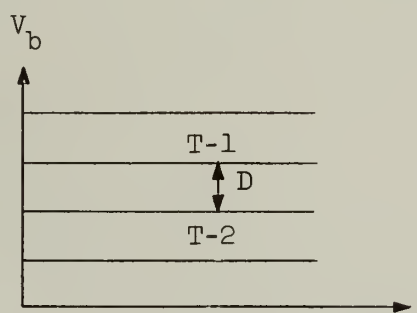


Figure 12

During the gating cycle, the two base voltages are somewhere within the shown tolerance bands. In the storing state these bands are shifted to a new DC

potential. If the system is to retain the state, the band separation D must be maintained at some minimum value. Hence, the velocity connected with the movement of the bands should ideally be the same for both bands. This means that the rise time of R_1 and R_2 should be very nearly the same. It does not state that the displacement of the bands be equal. It does, however, state that after reaching a steady state, there exists some minimum band separation. Hence the magnitude of the potential swing of R_1 and R_2 need not be equal.

Suppose the steady state criterion is met, but the rise times of R_1 and R_2 are not equal. Then the bands may overlap or cross, i.e. a change of state may occur if a steady state criterion is used. Does this mean that a loss of state occurs? This may be answered by considering two cases. The expression for the current gain is:

$$\alpha = \frac{\alpha_0 \epsilon^{-sm\tau}}{1 + s\tau}$$

m = delay constant (see transistor evaluation).

a) Attempted turn-off during $t < m\tau$

This situation exists during very fast gating cycles. The information is received at the emitter. The read-in gate is restored to its normal position before the collector responds to the change of state. The emitter network already reached a quasi-steady state since enough time ($\Delta_{B_{Max}}$) was allowed for settling. Charge redistribution occurs in the base region due to the diffusion network. As long as this process continues, the transistor cannot be considered off. If the back-bias is removed during this time interval, the stage retention is assured. The interval is computable from suitable experiments. The discharge time of the diffusion network is measurable as the turn-off time.

b) Attempted turn-off during $t > m\tau$

In this case the α-generator is already active. Since it has a delayed response, partially due to base transition times, the process is similar to that of the previous case, but in any case more favorable.

The above statements may be summarized as follows:

The state is stored on the emitter-base capacitance and possibly on the effective collector capacitance. The nonlinearity of the diffusion network is aiding in this problem. State retention is assured as long as reverse bias conditions on the conducting transistor do not persist longer than the turn-off time of the transistor under similar operating conditions.

Readout:

If the storage system is to be used for a register, the stored signal must be available upon demand. The collector current of T-2 is the stored information. One of the simplest methods to perform the gating function is that of using a current OR circuit.

$$I_{ST} \vee I_G = f_{OUT}$$

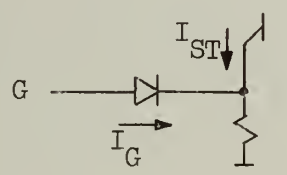


Figure 13

Conclusions:

The proposed storage element has the following properties:

1. It is a difference amplifier during gating. Its collector impedance is low to obtain fast settling responses.
2. It is a Schmitt-Trigger during storing.
3. Transition is accomplished by making use of the storage properties of transistors.

The proposed register system is characterized by:

1. using single-wire methods with only a single element in series with the signal path due to gate-in circuitry,
2. using no interconnecting logic within its own complex, but rather a system of signal busses from which information is transferred by using the drivers,
3. using a current OR circuit for its output gate to achieve high speed.

I. TRANSISTOR CHARACTERIZATION

One of the initial restrictions of the register system concerns the selection of transistors. It was considered that a somewhat cheaper type transistor than the GF45011 should be used. The N-100 and its complement, the N-101, were obtained in sample quantities from Texas Instruments, Inc. They are, however, not an experimental model, but have been in production for some time. A study of their static and dynamic characteristics was conducted, which is summarized in this section. The results of this section lead to the selection of the saturation margin, maximum current densities and to a general understanding of the device and its limitations. It is believed that this type of study is essential to any basic element design and useful, if not essential, in respect to estimated reliability and optimum switching speed.

A. DC Evaluation

Specifications for the NPN and PNP diffused-base germanium transistors are included on the enclosed specification sheet. The V_{EB} curves of Figure 14 and Figure 15 were obtained from measurements of V_{EB} vs. I_E for V_{CB} = 1v and 8v for a sample of Texas Instruments N-100 and N101's. The curves include the worst case values for the V_{BE} of the samples at the specified emitter currents. An additional variation of $\pm$0.025v is included at each point due to a temperature variation of from 15°C to 35°C, corresponding to an assumed temperature coefficient of 2.5 mv/°C. An additional variation of +20, -10 mv was added to compensate for aging.

N- 250 (DPNP) & N-251 (DNPN) Date 11-18-60

Customer University of Illinois

Specification for PNP & NPN Diffused Germanium Transistor Similar to T.I. N-100 & N-101

Mechanical Data

Metal case with glass-to-metal hermetic seal between case and leads. Unit weight is approximately 1 gram. These units meet JEDEC outline TO-5 and E3-44 base dimensions. The base is connected internally to the case.

Absolute Maximum Ratings at 25°C (case) temperature

Collector Current	50 ma
Base Current	10 ma
Total Device Dissipation in 25°C free air	150 mw
Collector Junction Temperature	100 °C
Storage Temperature Range	-65 °C to 100 °C

Electrical Characteristics at 25°C ambient temperature

Parameter	Test Conditions	Min.	Max.	Unit
I_{CBO}	V_{CB} = 10v, I_E = 0		8	μa
I_{EBO}	V_{EB} = 1v, I_C = 0		2	μa
I_{BX}	V_{CB} = 10v, V_{EB} = 1v		8	μa
BV_{CBO}	I_C = 100 μa, I_E = 0	30		v
BV_{EBO}	I_E = 100 μa, I_C = 0	7		v
BV_{CEX}	I_C = 100 μa, V_{BE} = .1v	30		v
h_{FE}	I_E = 10 ma, V_{CB} = 10v	30		v
V_{EB}	I_E = 10 ma, V_{CB} = 10v		0.4	v
h_{FE}	I_E = 15 ma, V_{CB} = 1v	20		
V_{EB}	I_E = 15 ma, V_{CB} = 1v		0.5	v
C_{ob}	V_{CB} = 10v, I_E = 0 ma, f = 1 mc		7	μμf
h_{fe}	V_{CE} = 10v, I_C = 10 ma, f = 100 mc	3db		

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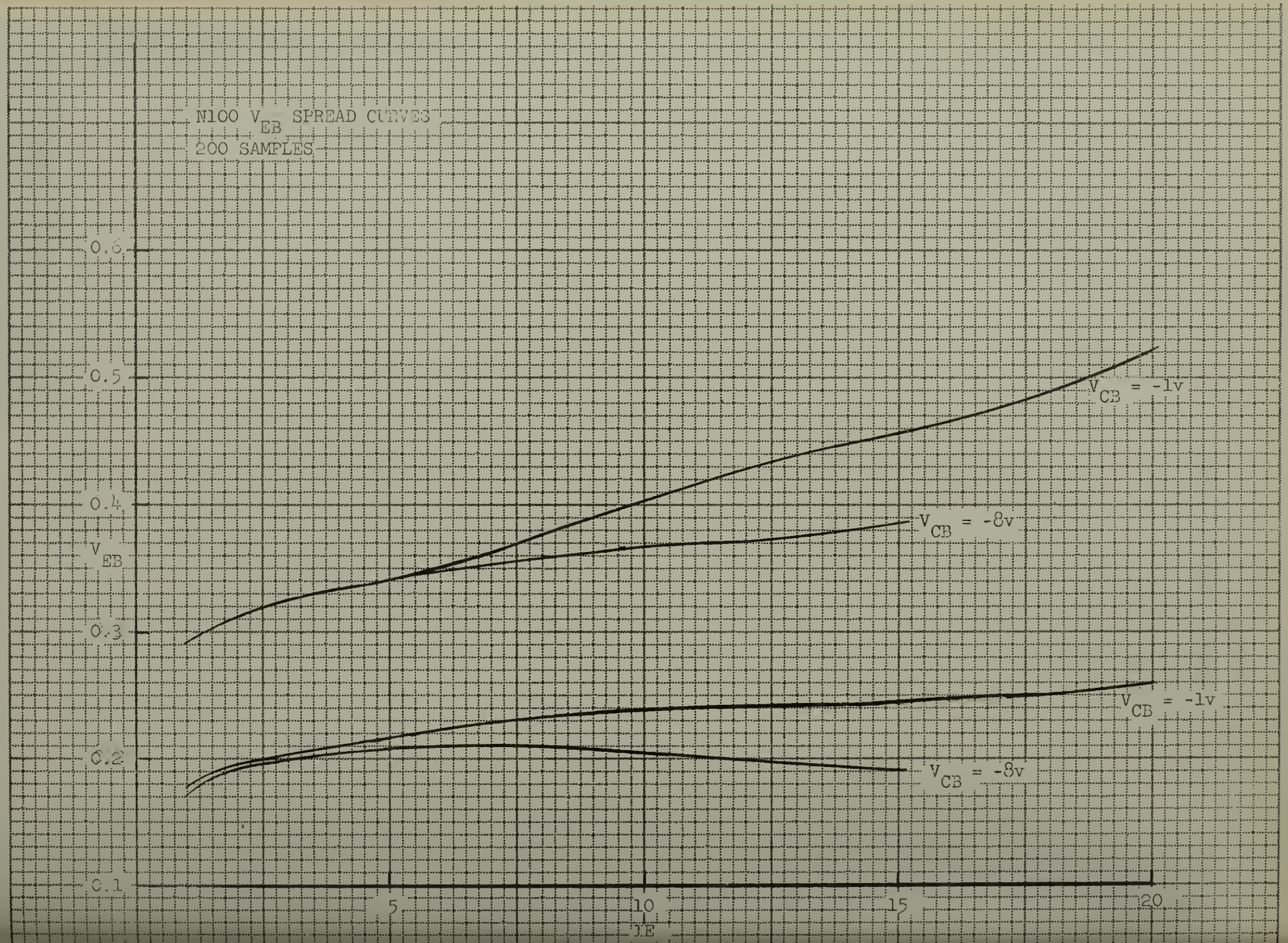

N100 V_{EB} SPREAD CURVES
200 SAMPLES
0.6
0.5
0.4
V_{EB}
0.3
0.2
0.1
5
10
15
20
IE
V_{CB} = -1v
V_{CB} = -8v
V_{CB} = -1v
V_{CB} = -8v

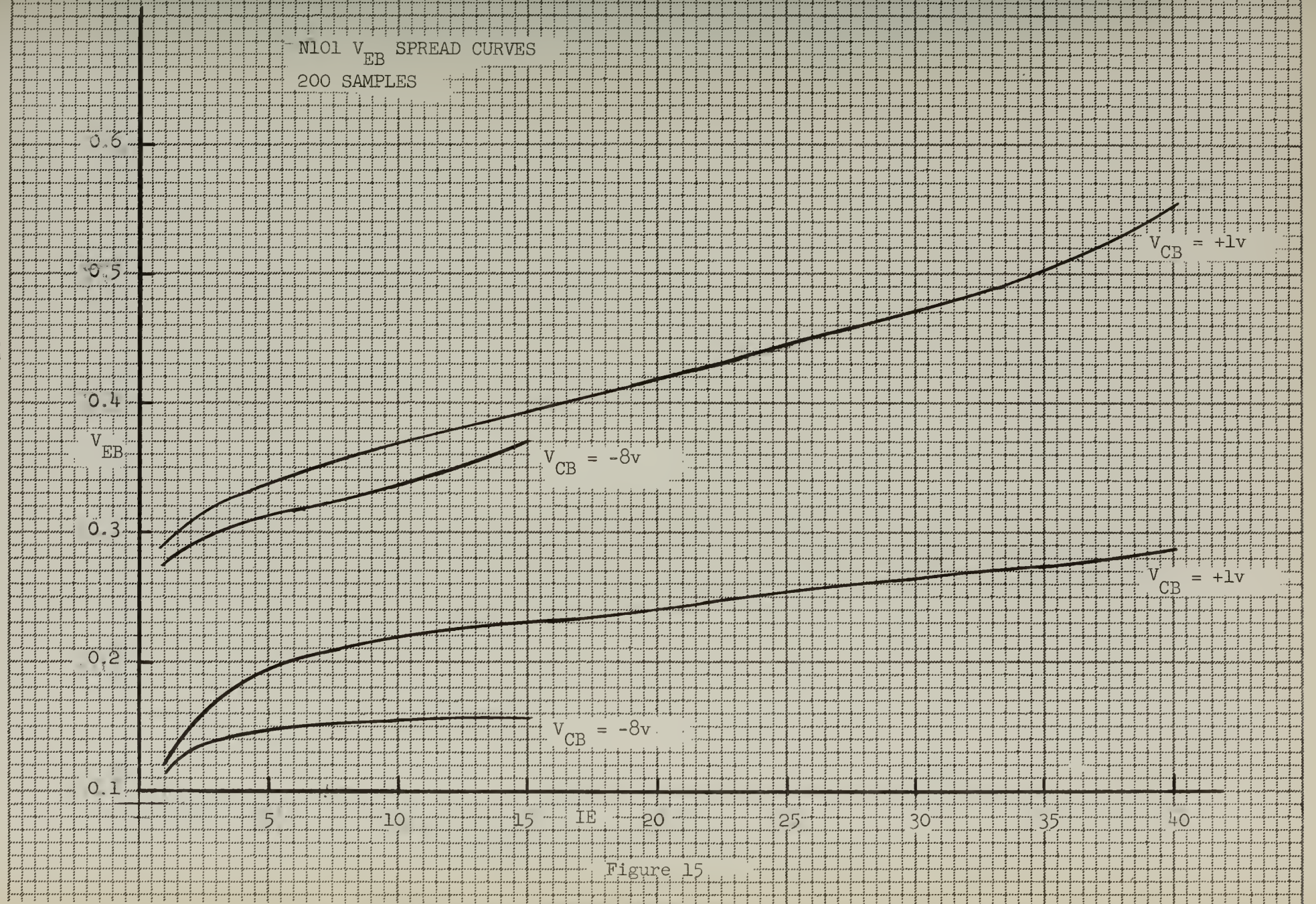
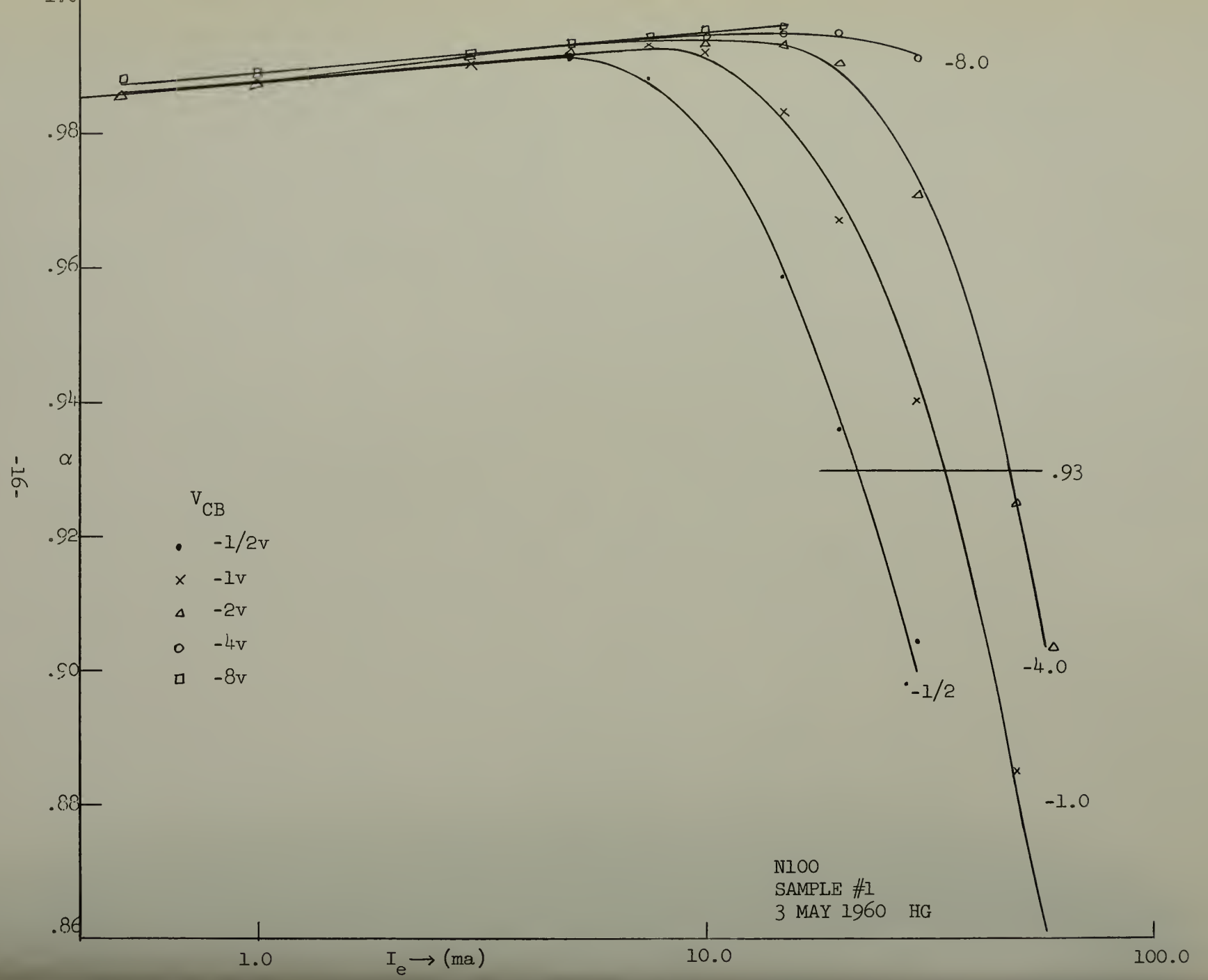

N101 V_{EB} SPREAD CURVES
200 SAMPLES
0.6
0.5
0.4
V_{EB}
0.3
0.2
0.1
V_{CB} = +1v
V_{CB} = -8v
V_{CB} = +1v
V_{CB} = -8v
5
10
15
IE
20
25
30
35
40

Figure 15


.98
.96
.94
α
.92
.90
.88
.86
V_{CB}
• -1/2v
× -1v
△ -2v
o -4v
□ -8v
-8.0
.93
-4.0
-1/2
-1.0
N100
SAMPLE #1
3 MAY 1960 HG
1.0
$I_e \rightarrow$ (ma)
10.0
100.0

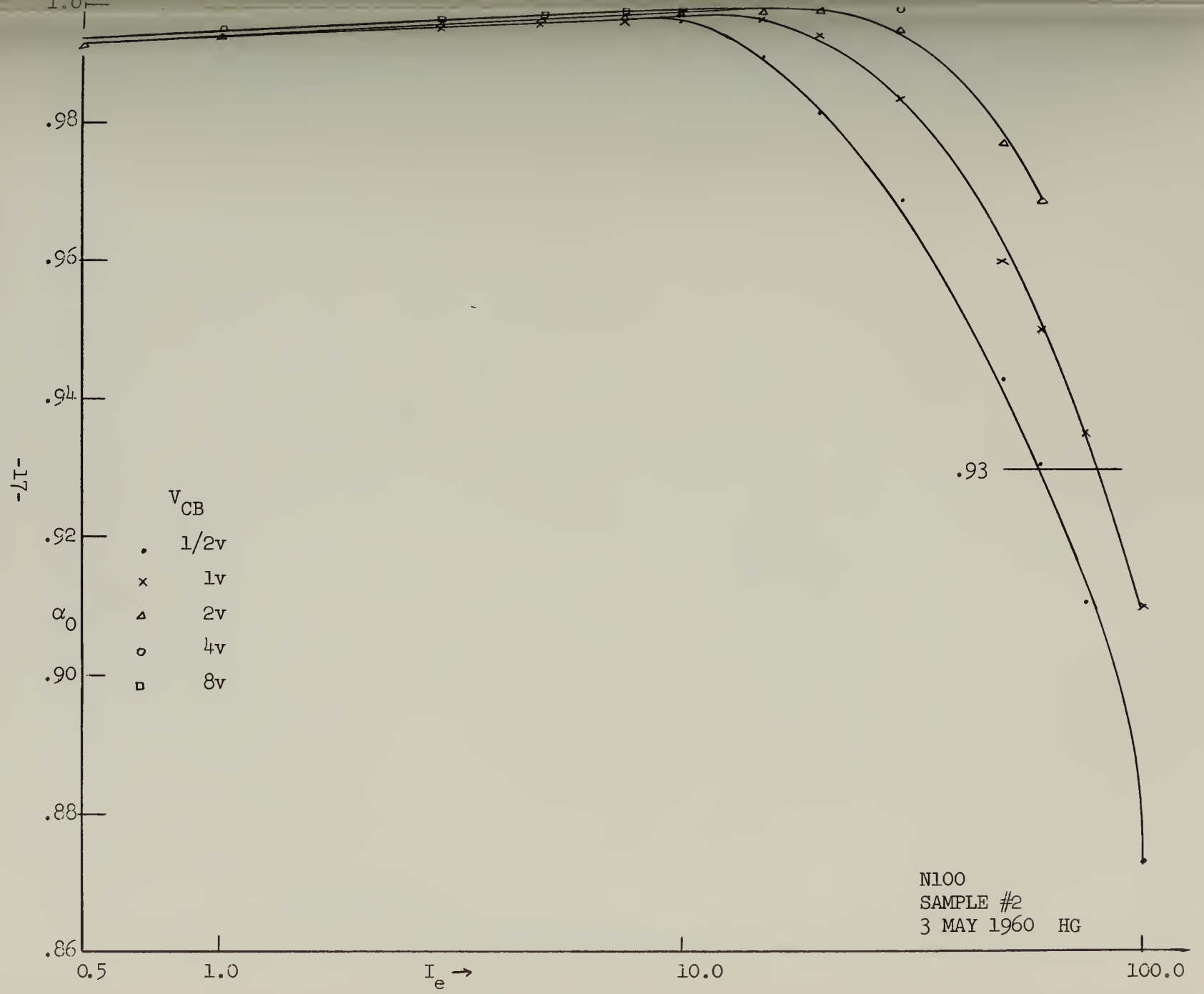

1.0
.98
.96
.94
.93
.92
.90
.88
.86
α_0
V_{CB}
1/2v
1v
2v
4v
8v
N100
SAMPLE #2
3 MAY 1960 HG
0.5
1.0
$I_e \rightarrow$
10.0
100.0

Figure 17

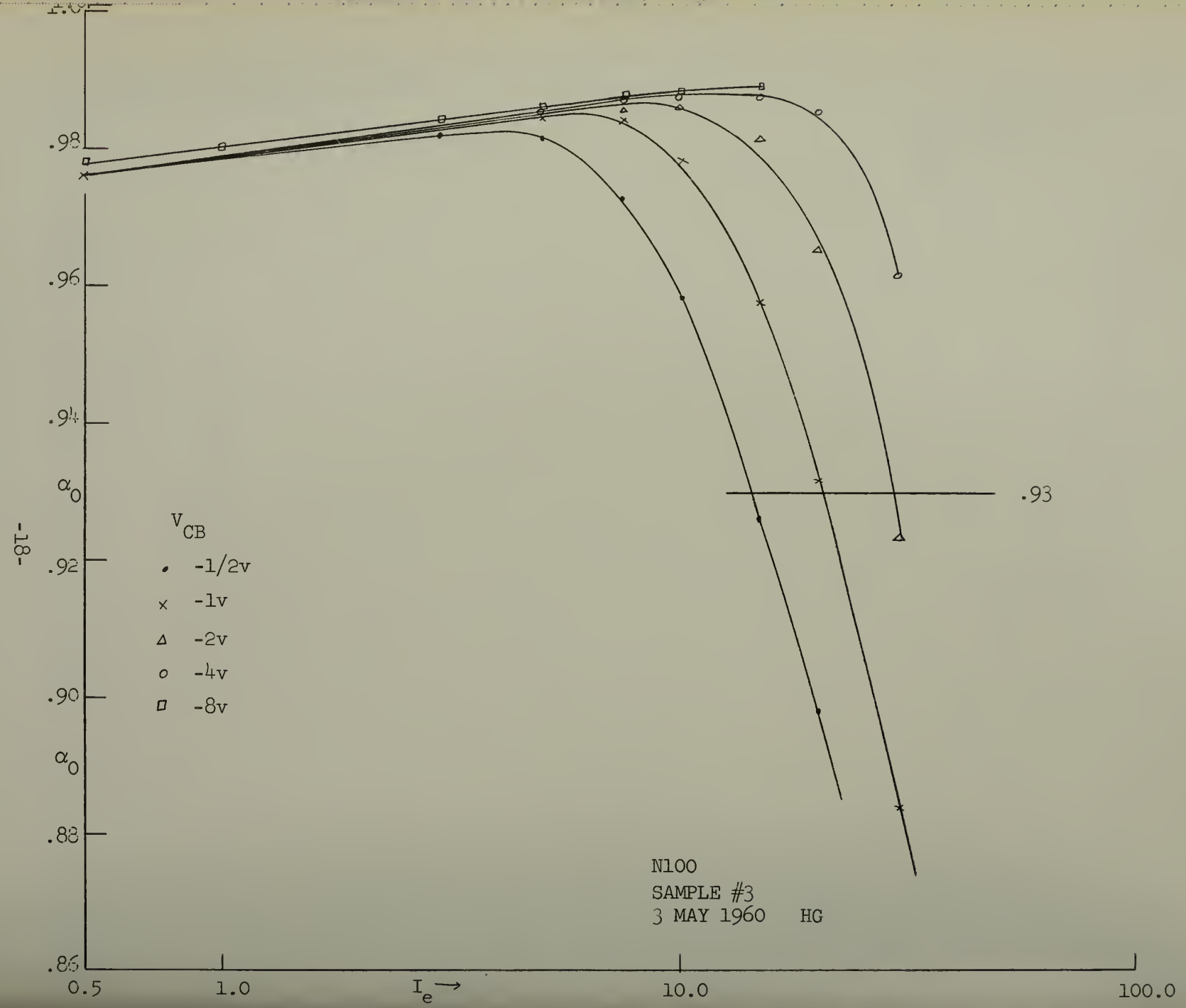

.98
.96
.94
α_0
.92
.90
α_0
.88
.86
.93
V_{CB}
-1/2v
-1v
-2v
-4v
-8v
N100
SAMPLE #3
3 MAY 1960 HG
0.5
1.0
$I_e \rightarrow$
10.0
100.0

Figure 18

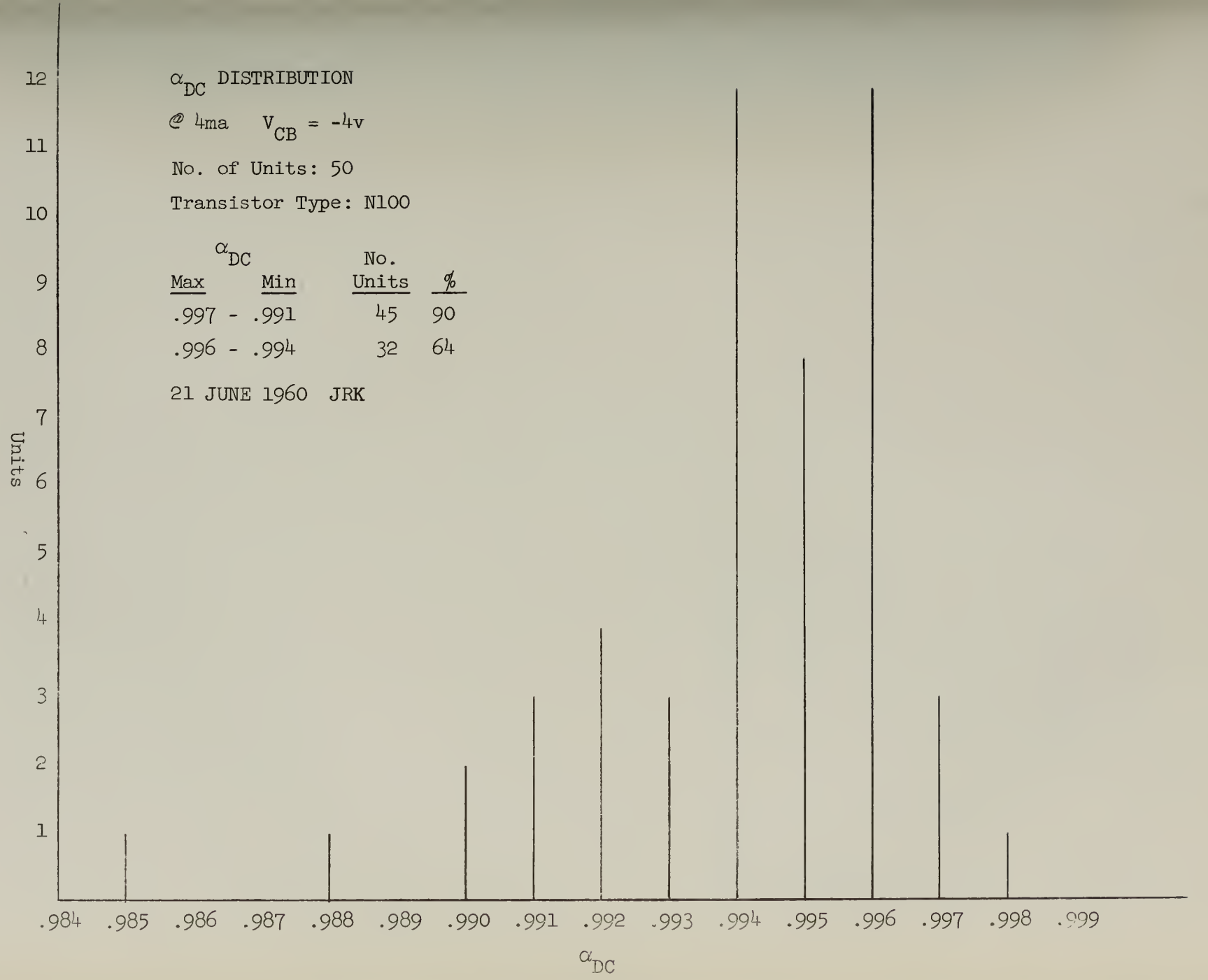

α_{DC} DISTRIBUTION
@ 4ma V_{CB} = -4v
No. of Units: 50
Transistor Type: N100
α_{DC} Max - Min | No. Units | %
.997 - .991 | 45 | 90
.996 - .994 | 32 | 64
21 JUNE 1960 JRK
Units
1
2
3
4
5
6
7
8
9
10
11
12
.984
.985
.986
.987
.988
.989
.990
.991
.992
.993
.994
.995
.996
.997
.998
.999
α_{DC}

Figure 19

V_{EB_f} DISTRICUTION @ 10ma

No. of Units: 50

Transistor Type: N100 (PNP)

Dev. Min	Dev. Max	V_{EB_f} Min	V_{EB_f} Max	No. Units	%
0	0	.280	.280	22	44
.010	.010	.270	.290	44	88
.005	.005	.275	.285	32	64
.010	.005	.270	.285	42	84

21 JUNE 1960 JRK

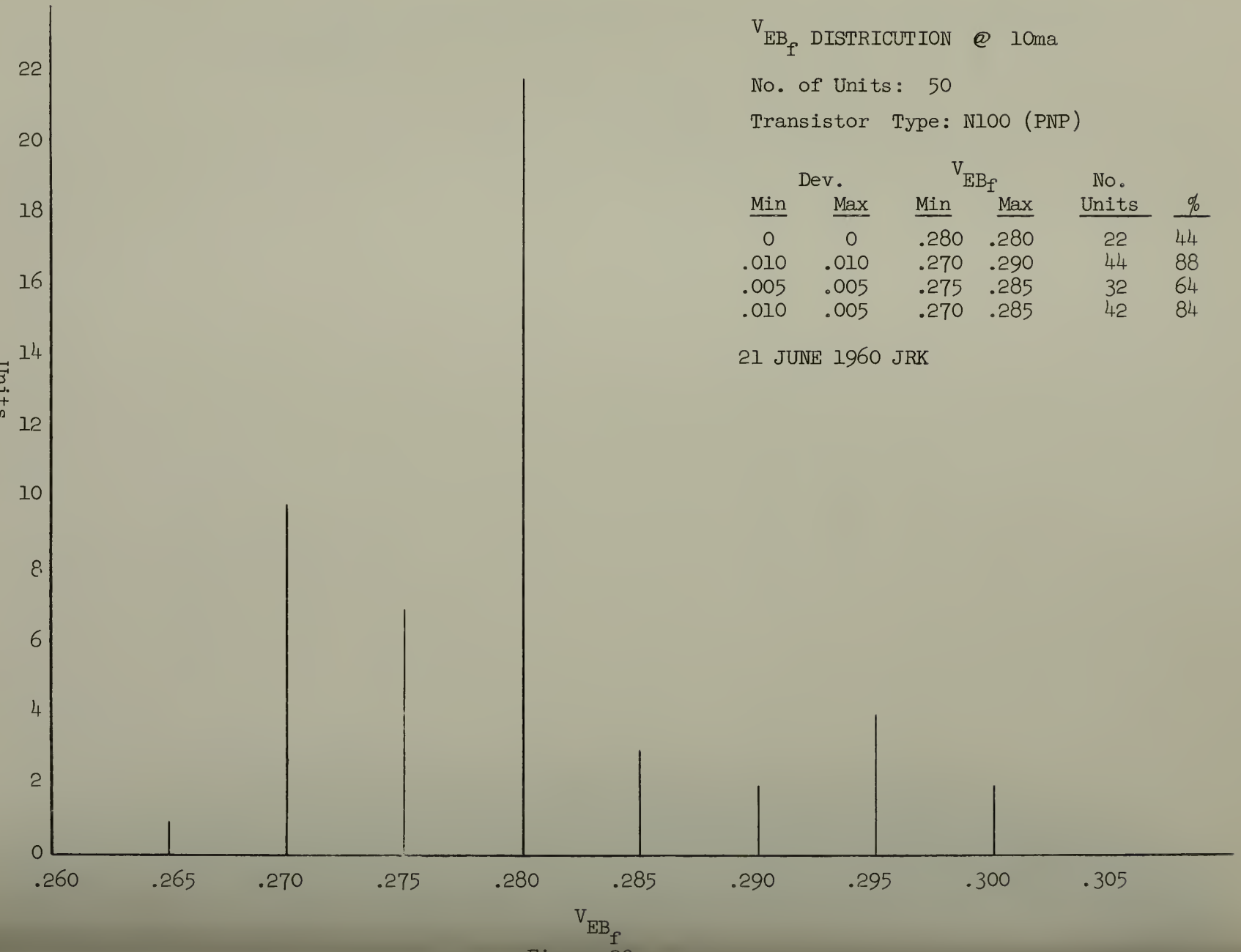


Figure 20

V_{EB_r} DISTRIBUTION @ 100 μa

No. of Units: 50

Transistor Type: N100 (PNP)

V_{EB_v} Min	No. Units	% > V_{EB_r}
5.4	1	98
6.0	5	88
6.4	1	86
7.0	4	61.8

21 JUNE 1960 JRK

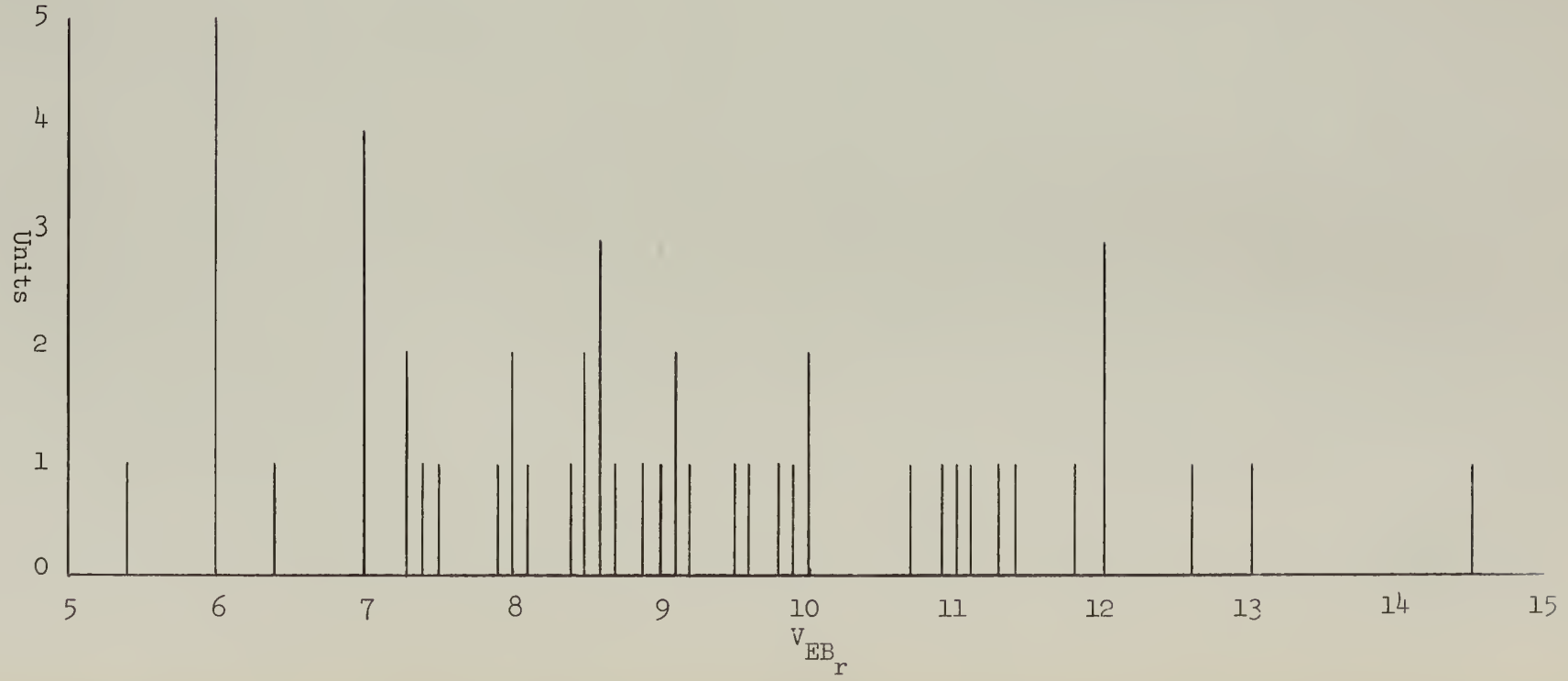
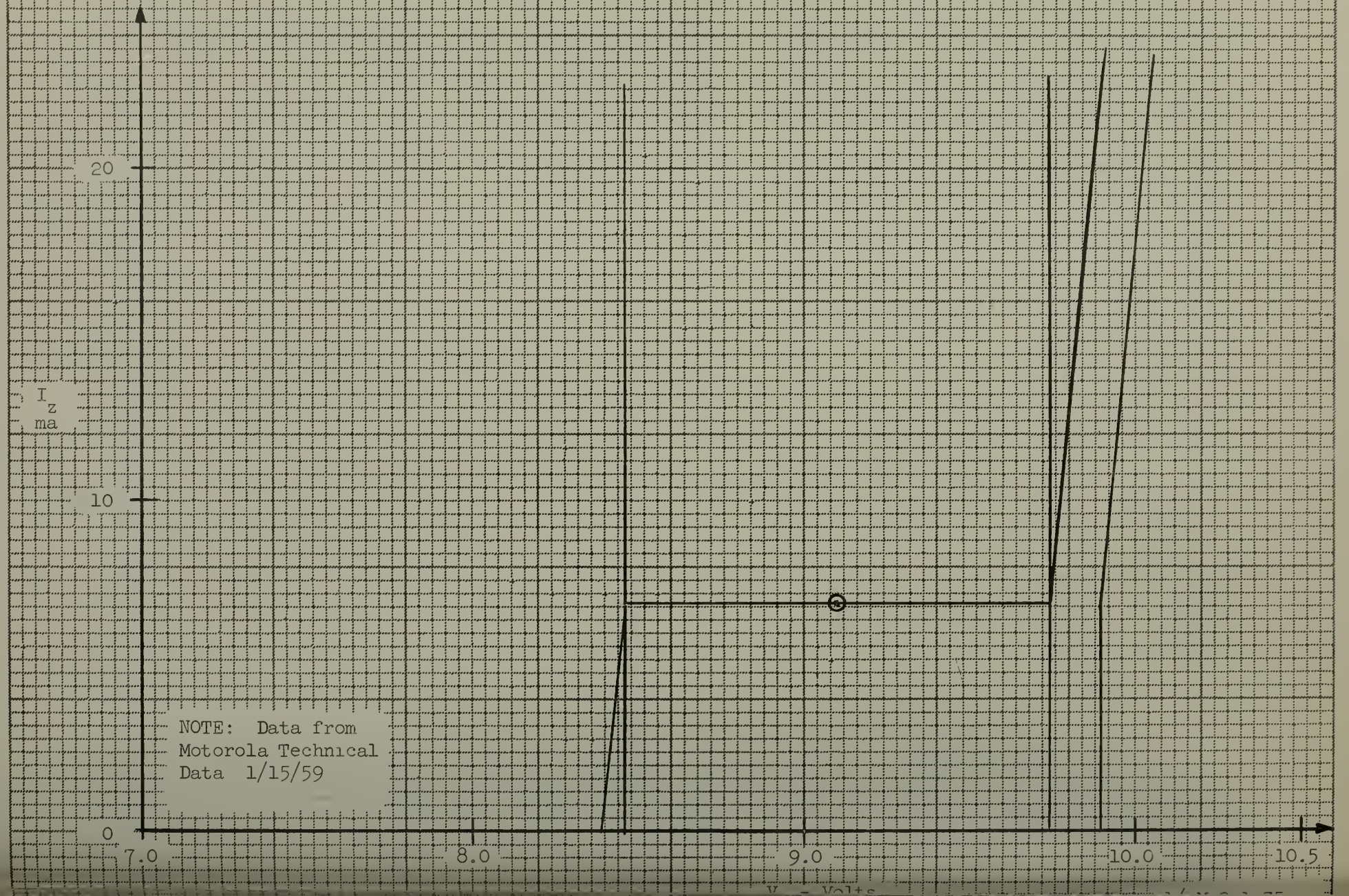


Figure 21


20
10
0
I_z ma
7.0
8.0
9.0
10.0
10.5
NOTE: Data from Motorola Technical Data 1/15/59

Of primary importance is the drop-off of α with emitter current. This is an indication of the saturation margin required at the anticipated emitter current. The curves of Figures 16 through 20 present an over-all view of the pertinent DC characteristics of N-100's. It is expected that the DC data for the N-101 would be similar, except the base to emitter diode drop, which is given separately.

B. AC Evaluation

In order to evaluate the switching speed of N-100 transistors in comparison with the GF45011 and S166 types, relative switching performance in a switching amplifier was measured. It was expected that there would be no significant difference in switching speed in an emitter-follower configuration. The testing circuit, shown below, is equivalent to the switching amplifier section in the standard circuits for the new Illinois computer, and about the same as that of the flowflop. V_{cc} was kept at a constant 19 volts when the turn-on speed was measured; it was adjusted to give the desired saturation margin for the turn-off speed measurement.

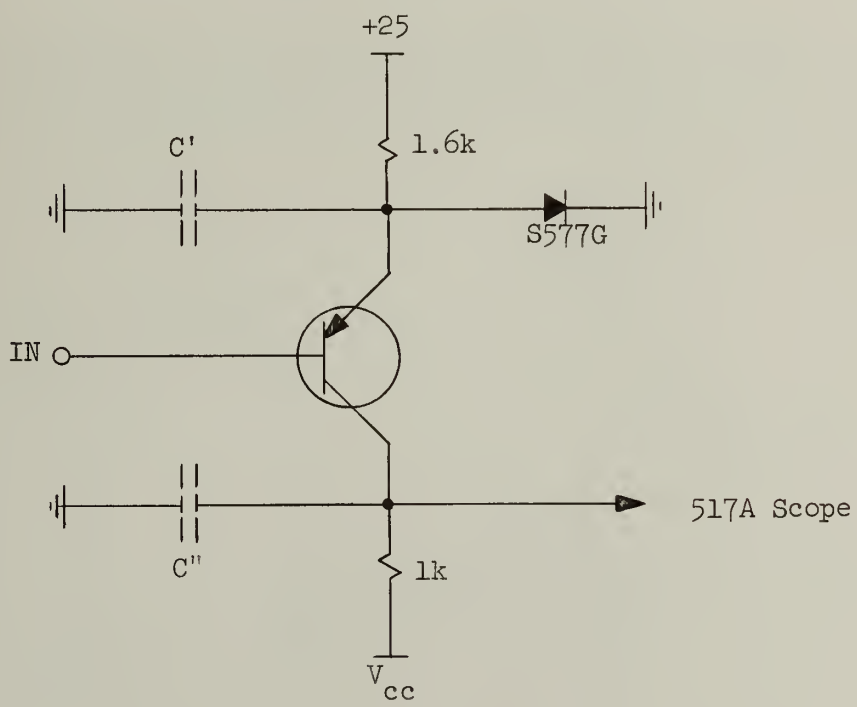


Figure 23
Switching Speed Test

Before describing the data, a brief theoretical analysis of the transient behavior will be included. A more complete account of switching behavior will be given elsewhere. Consideration of the turn-on transient leads to two different switching methods. If the switching diode is faster than the transistor, i.e. the recovery time of the diode is shorter than the switching time of the transistor, and if the enhancement current caused by C' at the emitter circuit is smaller than the magnitude of the constant current source, the circuit will respond like a current mode switching circuit. On the other hand, if the diode is slow or if the enhancement current exceeds the current source, the circuit will respond like a common emitter voltage amplifier with switched (or delayed) negative feedback at the emitter. For the first case the output voltage waveform at the collector will not overshoot. In the second case, the output waveform will show an overshoot unless the collector depletion layer capacitance C_c and the external stray capacitance C" is too large. For the circuit shown, the diode will recover in about 5 nanoseconds. The enhancement current is roughly:

$$i_{ENH} \approx \frac{C\,\Delta V}{\Delta t} = \frac{5 \times 4}{10} = 2 \text{ ma} \quad .$$

The current source is larger than this so that we are dealing with a current mode switch. The turn-off transient will be the same as the turn-on transient except for saturation effects at low base-to-collector voltages.

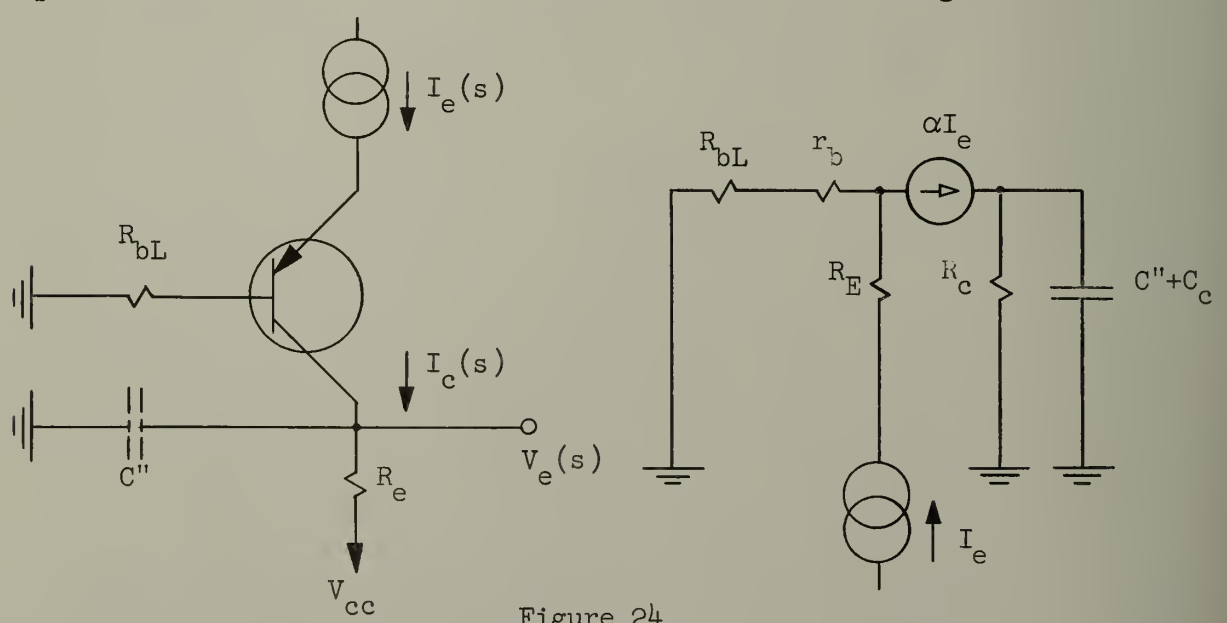


Figure 24

$$I_c(s) = \frac{R_b(1 + sC''R_c)}{R_c + R_b + sC''R_cR_b} I_e(s) + \frac{\alpha_o \tau \epsilon^{-sm\tau}(1 + sC''R_c)}{\tau - C_c(R_c + R_b) + sC''R_c(\tau - CR_b)} \frac{I_e(s)}{1 + s\tau}$$

$$- \frac{\dfrac{\alpha_o C_c \epsilon^{-sm\tau}(R_b + R_c + sC''R_bR_c)}{\tau - C_c(R_c + R_b) + sC''R_c(\tau - C_cR_b)} + \dfrac{R_b(1 + sC''R_c)}{R_c + R_b + sC''R_cR_b}}{1 + s[(C'' + C_c)R_c + C_cR_b] + s^2C''R_cC_cR_b} (1 + sC''R_c)I_e(s) \qquad (1)$$

$$V_c(s) = \frac{R_c}{1 + sC''R_c} I_e(s)$$

$$V_c(s) = \frac{R_bR_c}{R_c + R_b + sC''R_cR_b} I_e(s) + \frac{\alpha_o \tau \epsilon^{-sm\tau} R_c}{\tau - C_c(R_c + R_b) + sC''R_c(\tau - C_cR_b)} \frac{I_e(s)}{1 + s\tau}$$

$$- \left(\frac{\alpha_o C_c \epsilon^{-sm\tau}(R_b + R_c + sC''R_bR_c)}{\tau - C_c(R_c + R_b) + sC''R_c(\tau - C_cR_b)} + \frac{R_b(1 + sC''R_c)}{R_c + R_b + sC''R_cR_b} \right) R_c$$

$$\times \frac{I_e(s)}{1 + s[(C_c + C'')R_c + C_cR_b) + s^2C''R_cC_cR_b} \qquad (2)$$

where:

$$\alpha = \frac{\alpha_o \epsilon^{-sm\tau}}{1 + s\tau} = \alpha_o \frac{\epsilon^{-\frac{1-K}{K}\frac{s}{\omega_\alpha}}}{1 + \frac{s}{\omega_\alpha}} \qquad (3)$$

$R_b = R_{bL} + r_b'$

C_c = collector layer depletion capacitance

K = phase factor .

In order to obtain the main terms, the following assumptions are made:

$$R_b \ll R_c$$

$$sC_cR_b \ll 1$$

$$sC''R_b \ll 1 \quad .$$

This yields:

$$V_c(s) = R_bI_e(s) + \frac{\alpha_o\tau R_c \epsilon^{-sm\tau}}{\tau - C_cR_c + sC''R_c\tau} \frac{I_e(s)}{1 + s\tau}$$

$$- \left(\frac{\alpha_o R_c^2 C_c \epsilon^{-sm\tau}}{\tau - C_cR_c + sC''R_c\tau} + R_b \right) \frac{I_e(s)}{1 + s(C_c + C'')R_c} \qquad (4)$$

For a step input, the time domain solution is:

$$v_c(t) = R_bI_e\epsilon^{-t/T} + \frac{\alpha_o I_e R_c \tau}{\tau - (C_c + C'')R_c} (1 - \epsilon^{-(t-m\tau/T)})U(t - m\tau)$$

$$- \frac{\alpha_o I_e R_c R_c(C_c + C'')}{\tau - (C_c + C'')R_c} (1 - \epsilon^{(t-m\tau/R_c C_c + C'')}) U(t - m\tau)$$

$$v_c(t) = R_bI_e\epsilon^{-t/T} + \frac{\alpha_o I_e R_c \tau}{\tau - T} (1 - \epsilon^{-(t-m\tau/T)}) U(t - m\tau)$$

$$- \frac{\alpha_o I_e R_c T}{\tau - T} (1 - \epsilon^{-(t-m\tau/\tau)}) U(t - m\tau) \qquad (5)$$

where

$$T = (C_c + C'')R_c \quad .$$

If the exponentials are approximated by linear segments, the following diagrams represent the two cases:

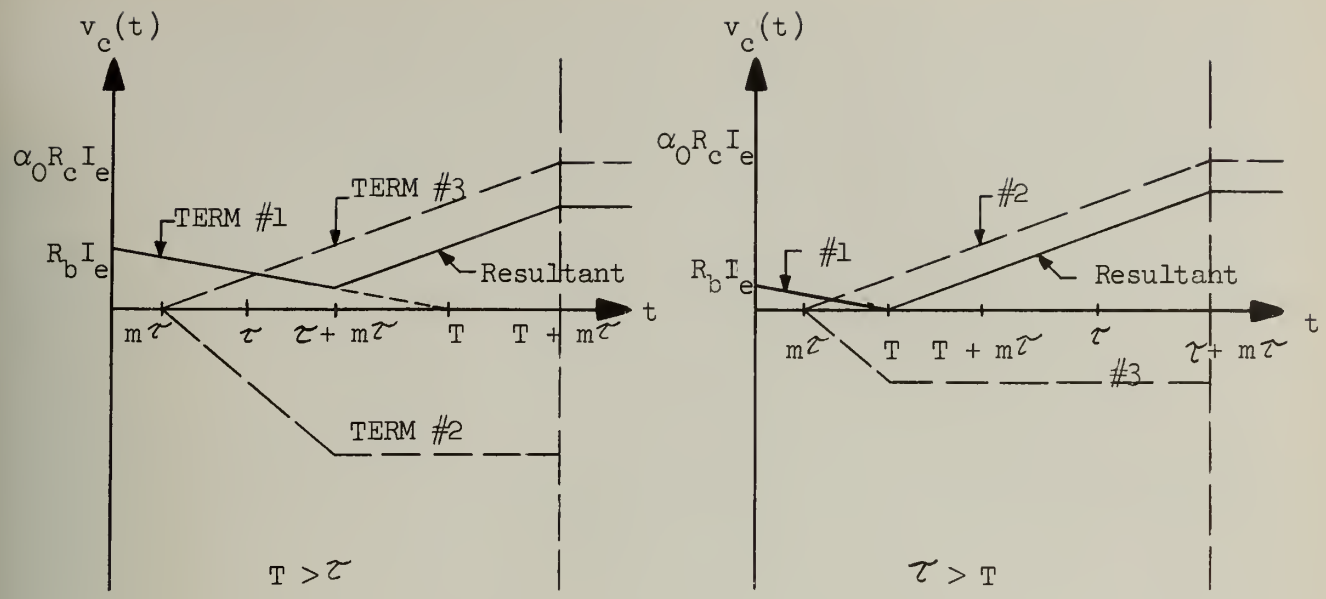


Figure 25

For the capacity-controlled circuit ($T > \tau$) the output waveform is approximated by an exponential curve with time constant $T - \tau$ and with delay time $\tau(1+m)$. For the cut-off frequency controlled circuit ($\tau > T$) the output waveform is approximated by an exponential curve with time constant $\tau - T$ and delay time $T + m\tau$. In the actual circuit $I_e(s)$ is generated by the base input voltage. This causes a passive feedthrough effect as discussed in the following section.

$$v_c'(t) = -\frac{C_c E_B}{C_c + C''} \epsilon^{-t/T} \quad . \tag{6}$$

The output voltage is therefore given by:

$$v_c''(t) = (R_b I_e - \frac{C_c}{C_c + C''} E_B) \epsilon^{-t/T} + \alpha_o I_e R_c (1 - \quad -(t-m\tau/\tau)} U(t - m\tau) \tag{7}$$

For the turn-off transient, the delay due to saturation must be added to (7). Evaluation for N-100, GF45011 and S166 yielded the following data:

TYPE	C_c	C"	R_c	T(nsec)	$f_\alpha(M_c)$	τ(nsec)	$(1+m)\tau$	$2.2(T-\tau)$	Observed t_r
N-100	7	4	1	11	150	1.11	2.5	22	22
GF45011	3	4	1	7	500	0.33	.75	14.5	14
S166	2	4	1	6	500	0.33	.75	12.5	12

C_c = maximum value specified

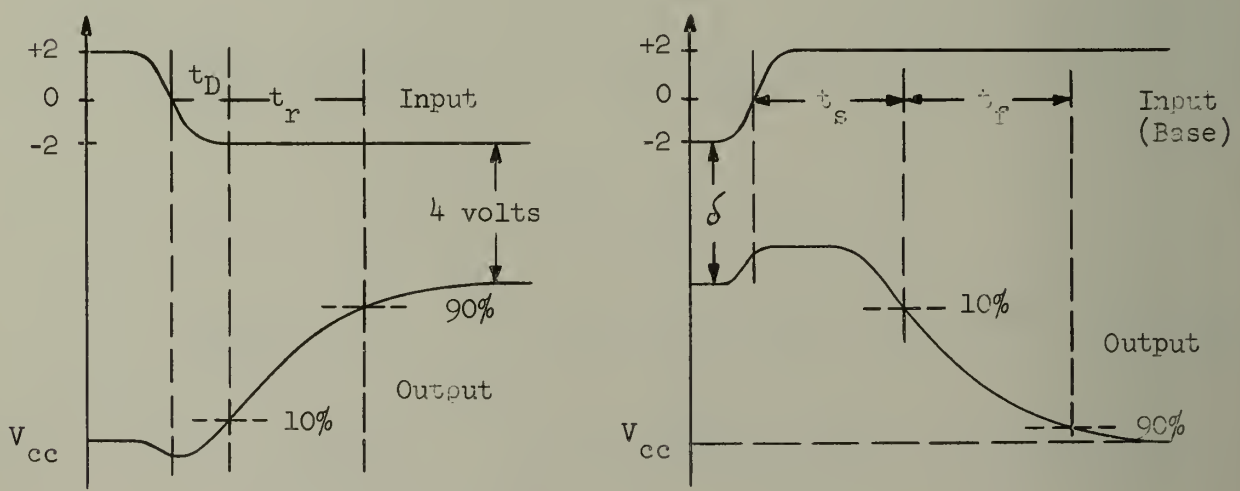
C" = Input capacity of 517A ($\sim$ 300F)

$m = n = \frac{1-K}{K}$ $\quad K = 0.4$

t_r = 10% - 90% .

The agreement between calculated and observed rise time is good. It may be concluded that the inverse gain-bandwidth product of the N-100 is 50% larger than that of the GF45011.

Observed Waveforms:



a) Turn-On

Figure 26

TYPE	α_0	Turn On		δ = 0.5v		δ = 0.8v		δ = 1.0v		δ = 2.0v		δ = 1.5v	
		t_D	t_r	t_s	t_f	t_s	t_f	t_s	t_f	t_s	t_f	t_s	t_f
	.998	3	22	22	24	12	26	8	26	4	26	5	26
N-100	.988	3	22	47	25	34	25	32	25	8	26	14	26
	.986	3	22	51	30	36	28	32	26	8	26	14	26
	.992	1.5	14	2.5	24	2	22	2	22	2	22	--	--
GF45011	.978	1.5	15.5	4	25	3	23	2	22	2	22	--	--
	.971	1.5	15.5	4	25	3	23	2	22.5	2	22	--	--
	.992	1.5	12	7	22	4	22	3	22	2	22	--	--
S166	.981	1.5	13.5	7	23	4	22	3	22	2	22	--	--
	.979	1.5	14	10	22	5	22	4	22	2	22	--	--

From the data the following conclusions are drawn:

1. The S166 is slightly faster than the GF45011 in the turn-on condition. This is probably due to the smaller depletion layer capacitance.
2. The S166 has a larger carrier storage than the GF45011, thereby requiring a larger saturation margin.
3. The N-100 has large carrier storage. The saturation margin should be greater than 2.0 volts. The dependence of t_s on α_0 is obvious from the Ebers-Moll theory..

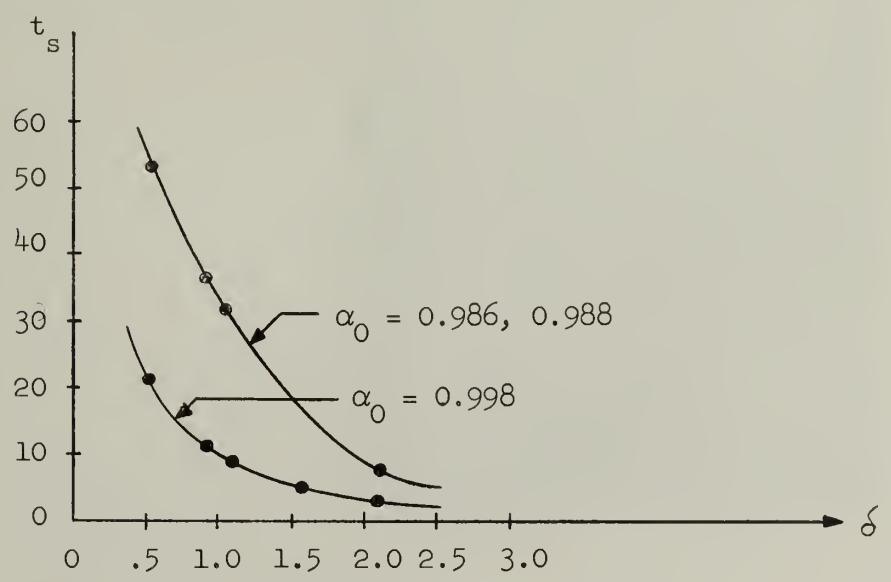
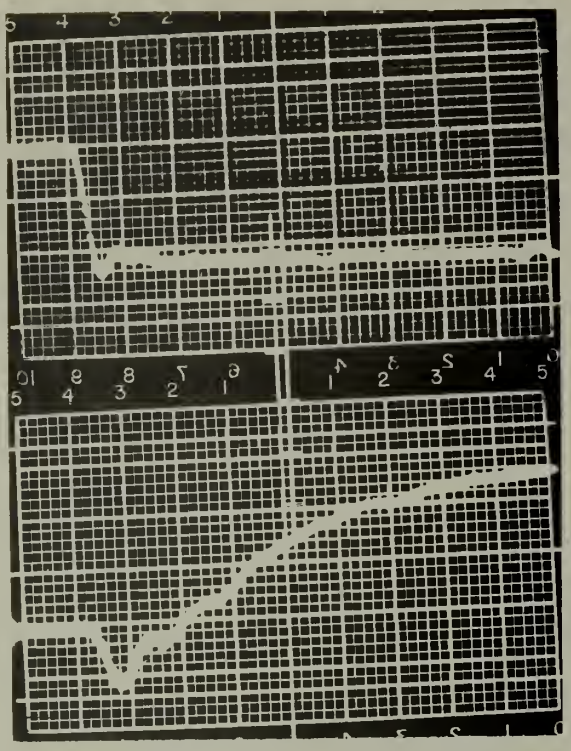


Figure 27

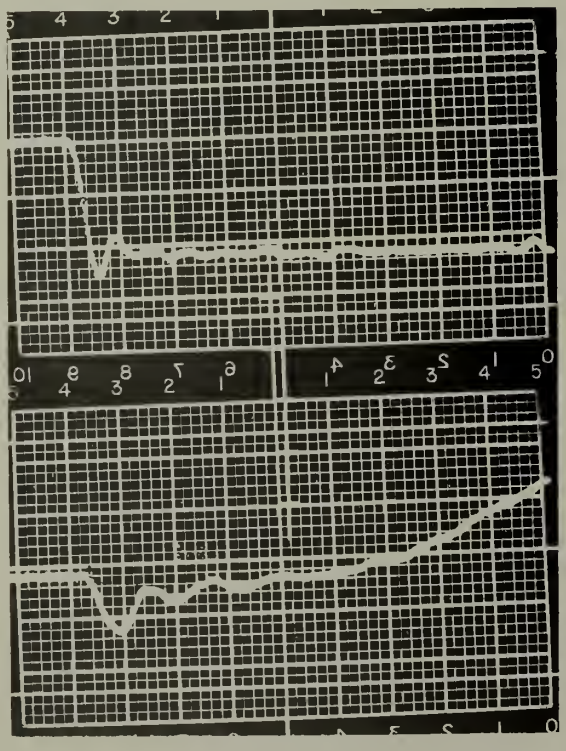


Turn-on Transient

2nsec/cm 2v/cm

GF45011

Figure 28a



N-100

Figure 28b

Base Input Impedance (for Emitter Follower):

A simplified analysis is given here to theorize the correct value of a speed-up capacitor.

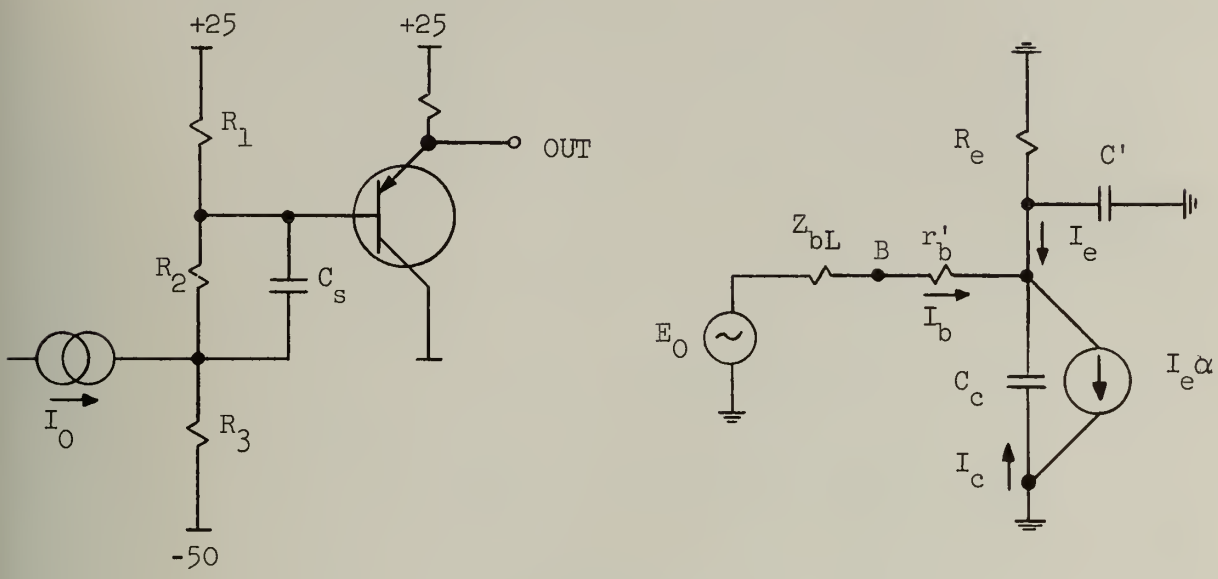


Figure 29

Base Input Impedance:

$$Z = r'_b + R_e \frac{1 + s\tau}{(1 + sT)(1 + s\tau) - \alpha'_0(1 + sT')}$$

$$\alpha = \frac{\alpha'_0}{1 + s\tau} = \frac{\alpha_0 \epsilon^{-sm\tau}}{1 + s\tau}$$

$$T = R_e(C_c + C') \qquad T' = R_eC'$$

$$Z = r'_b + \frac{R_e}{1 - \alpha'_0} \frac{1 + s\tau}{1 + s\frac{T + \tau - \alpha'_0T'}{1 - \alpha'_0} + s^2 \frac{T\tau}{1 - \alpha'_0}}$$

In order to evaluate the equation, two cases are considered:

Case I: $t < m\tau$ $\qquad \alpha'_0 = 0$

$$Z = r'_b + \frac{R_e}{1 + sT}$$

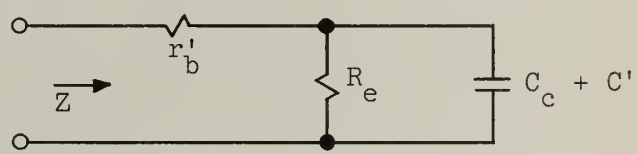


Figure 30

Case II: $t > m\tau \qquad \alpha_0' = \alpha_0$

$$Z = r_b' + \frac{R_e}{1 - \alpha_0} \quad \frac{1 + s\tau}{1 + s\,\dfrac{T + \tau - \alpha_0 T'}{1 - \alpha_0} + s^2\,\dfrac{T\tau}{1 - \alpha_0}}$$

$$Z = r_b' + \frac{R_e}{1 - \alpha_0}\left(\frac{A}{1 + sT_1} + \frac{B}{1 + sT_2}\right)$$

$$T_1 \simeq \frac{T\tau}{T + \tau - \alpha_0 T'}$$

$$T_2 \simeq \frac{T + \tau - \alpha_0 T'}{1 - \alpha_0} > T_1$$

$$A \simeq \frac{\tau - T_1}{T_2 - T_1} \begin{matrix} > \\ < \end{matrix} 0$$

$$B \simeq \frac{T_2 - \tau}{T_2 - T_1} > 0$$

The circuit can therefore be reduced to:

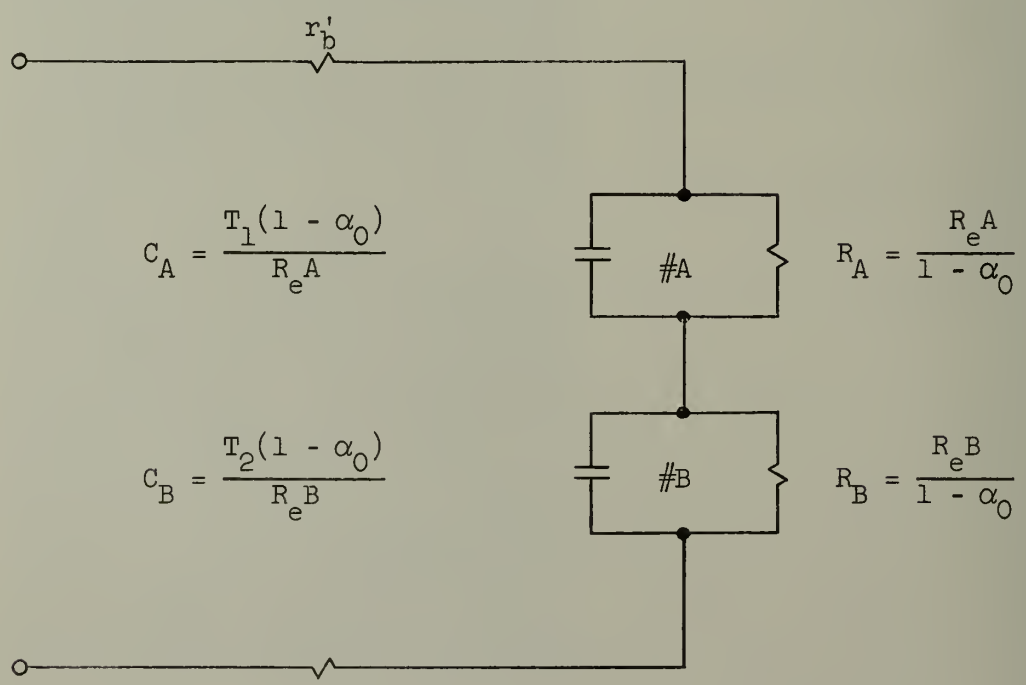


Figure 31

It is to be noted that the network A may have a negative resistance if

$$\tau - T_1 < 0$$

$$\tau - \frac{T\tau}{T + \tau - \alpha_0 T'} = \tau\left(\frac{\tau - \alpha_0 T'}{T + \tau - \alpha_0 T'}\right) < 0$$

i.e. $\tau - \alpha_0 R_e C' < 0$.

This condition was discussed in detail in an earlier report. Comparison of circuits A and B yields:

$$\frac{A}{B} = \frac{\tau - T_1}{T_2 - \tau} = \frac{\tau - \frac{T\tau}{T + \tau - \alpha_0 T'}}{\frac{1}{1 - \alpha_0}(T + \tau - \alpha_0 T') - \tau}$$

$$< (1 - \alpha_0)\frac{\tau(\tau - \alpha_0 T')}{(T + \alpha_0\tau - \alpha_0 T')^2}$$

$$< (1 - \alpha_0) .$$

Hence the network A may be neglected. Consideration of B yields:

$$B = \frac{(T - \alpha_0 T' + \alpha_0\tau)(T - \alpha_0 T' + \tau)}{(T + \tau - \alpha_0 T')^2 - (1 - \alpha_0)T\tau} \simeq 1 \qquad (1 - \alpha_0 \ll 1)$$

$$T_2 = \frac{1}{1 - \alpha_0}[R_e(C_c + (1 - \alpha_0)C') + \tau] .$$

The resulting equivalent for $t > m\tau$ is then:

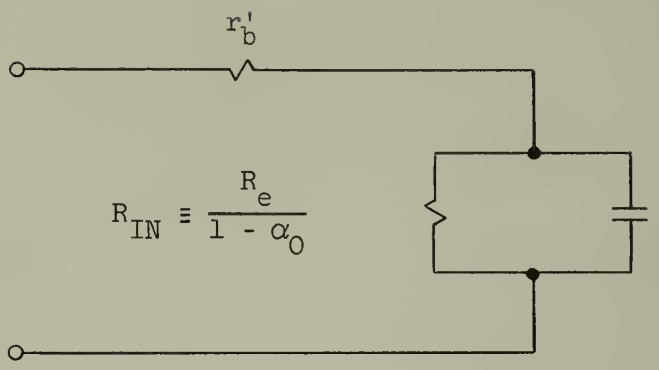


Figure 32

Due to the phase factor of α the over-all equivalent circuit will be somewhere between the circuits discussed in Cases I and II. In order to get a good approximation, α_0 in the last equivalent circuit may be taken slightly smaller than the actual value. Two methods seem justifiable:

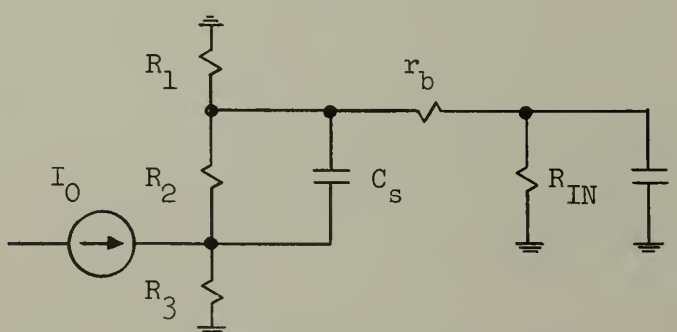
a) $\alpha_{OM} = \dfrac{\alpha_0 t_r}{t_r + t_d}$

t_r = rise time

t_d = delay time

b) $\alpha_{OM} = m\alpha_0$.

Calculation of peaking capacitor:



α_{OM} = Modified α_0

$R_{IN} = \dfrac{R_c}{1 - \alpha_{OM}}$

$C_{IN} = C_c + (1 - \alpha_{OM})C' + \dfrac{\tau}{R_e}$

Figure 33

For a collector clamped by bumping diodes, the following circuit may be used:

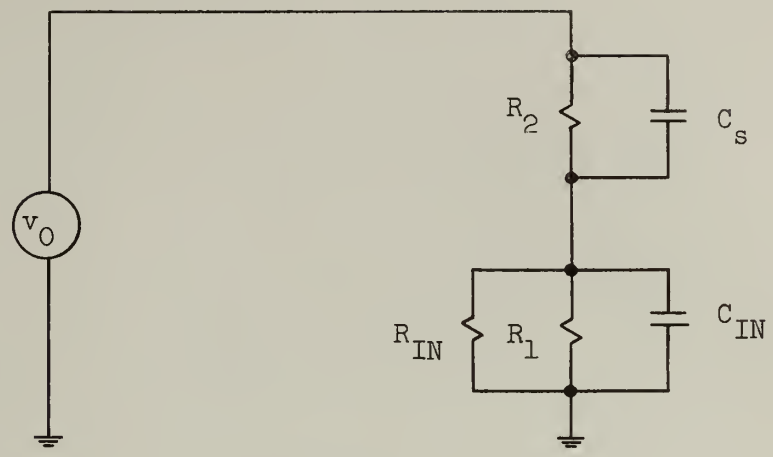


Figure 34

The optimum value of C_s is given by:

$$C_s = \frac{R_1 R_{IN}}{R_2(R_1 + R_{IN})} \quad .$$

Example: Standard circiuts bleeder:

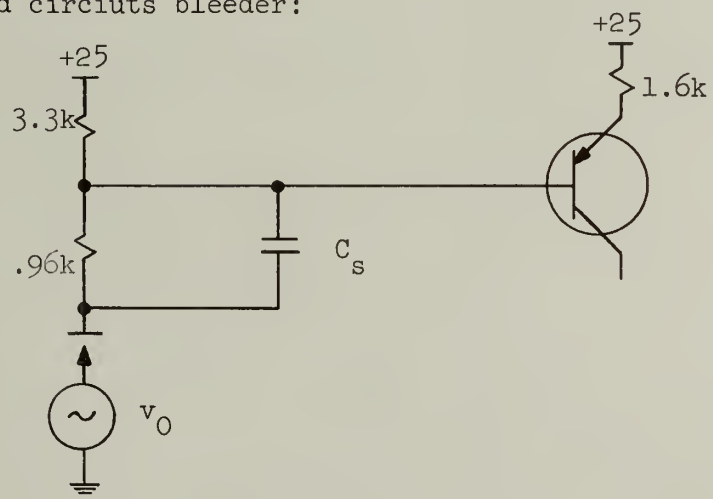


Figure 35

$$\alpha_{OM} = \frac{.93 \cdot 2}{1 + 2} = .62$$

$$R_{IN} = \frac{1.6}{1 - 0.62} = 4.2k$$

$$C_{IN} = C_c + (1 - \alpha_{OM})C' + \frac{\tau}{R_e} = 3 + 3.8 + \frac{0.3}{1.6}$$

$$= 7 \ \mu\mu f$$

$$C_s = \frac{3.3 \cdot 4.2 \cdot 7}{0.96(3.3 + 4.2)} = 13.5 \ \mu\mu f$$

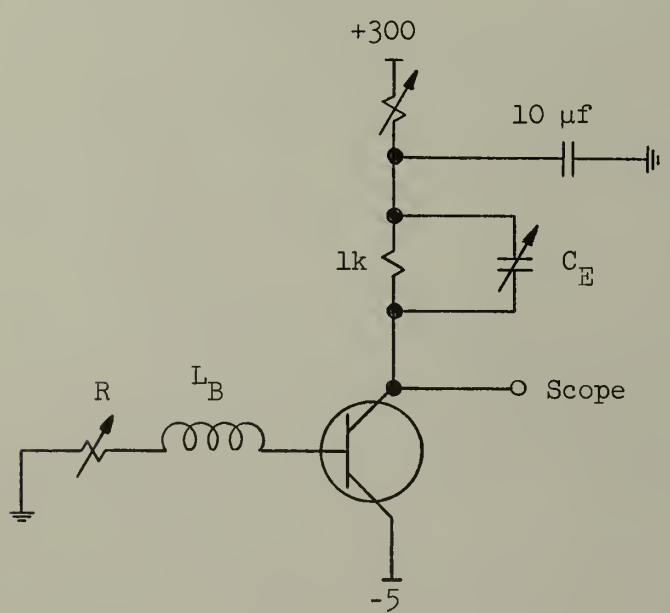
$$C'_s = \frac{3.3 \cdot 7}{.96} = 20.4 \ \mu\mu f \quad (R_{IN} = \infty) .$$

For optimum waveform transmission C_s should be between 13.5 and 20.4 $\mu\mu f$. An experiment was conducted to check these results and appeared to verify the above statements.

If design calculations are made on the basis of the above work it should be remembered that a) as the emitter current increases τ becomes larger and α_{OM} smaller. Hence the size of the speed-up capacitor increases rapidly. b) If diode clamping circuits are used at the base C_{IN} should include the capacitance of the clamping network.

Stability Considerations:

In order to estimate the behavior of the N-100 in the negative real input impedance region, the following test was conducted to measure the negative real part of z_{11}:



Note: R is adjusted to get threshold of oscillations.

Figure 37

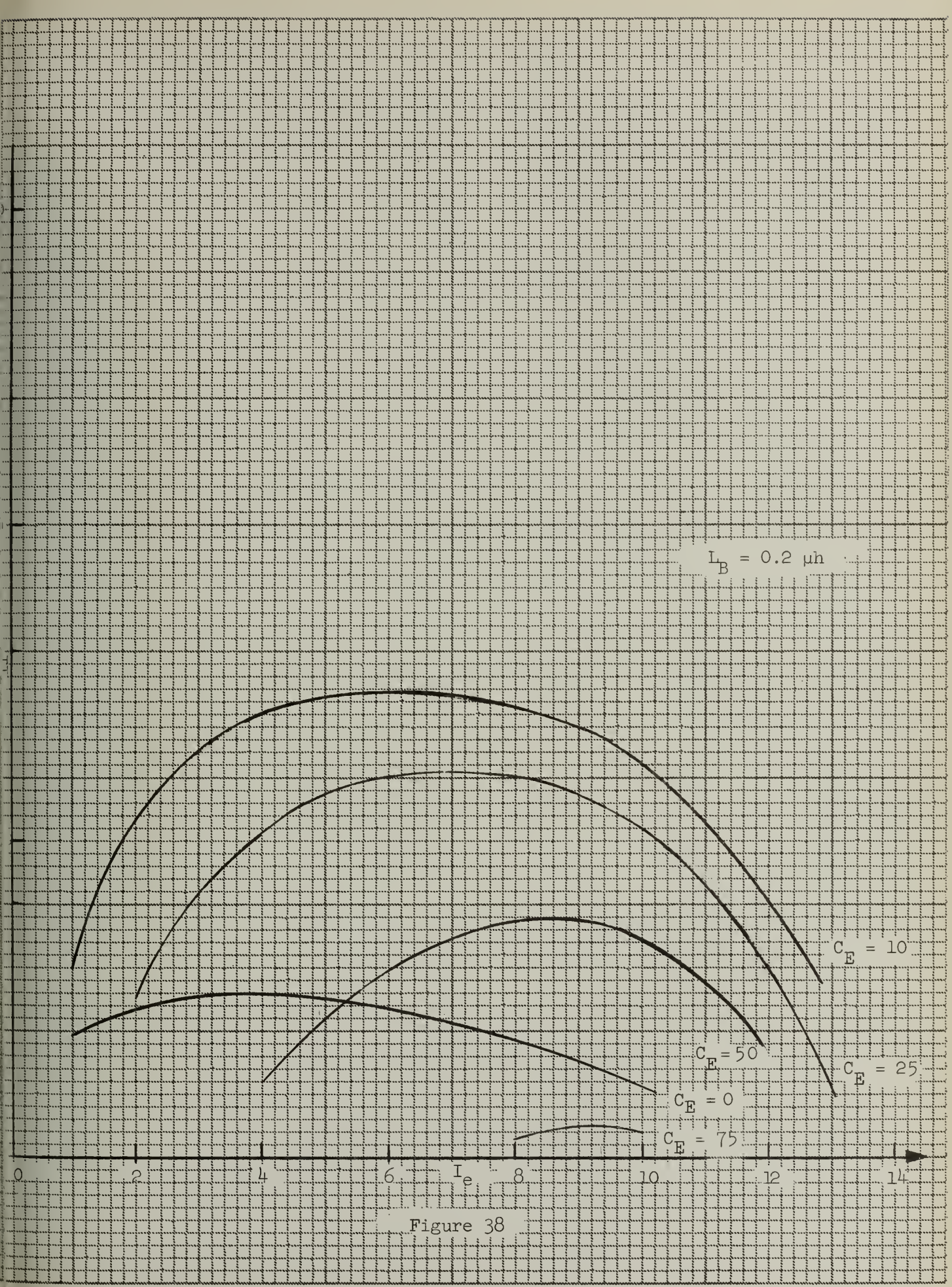


Figure 38

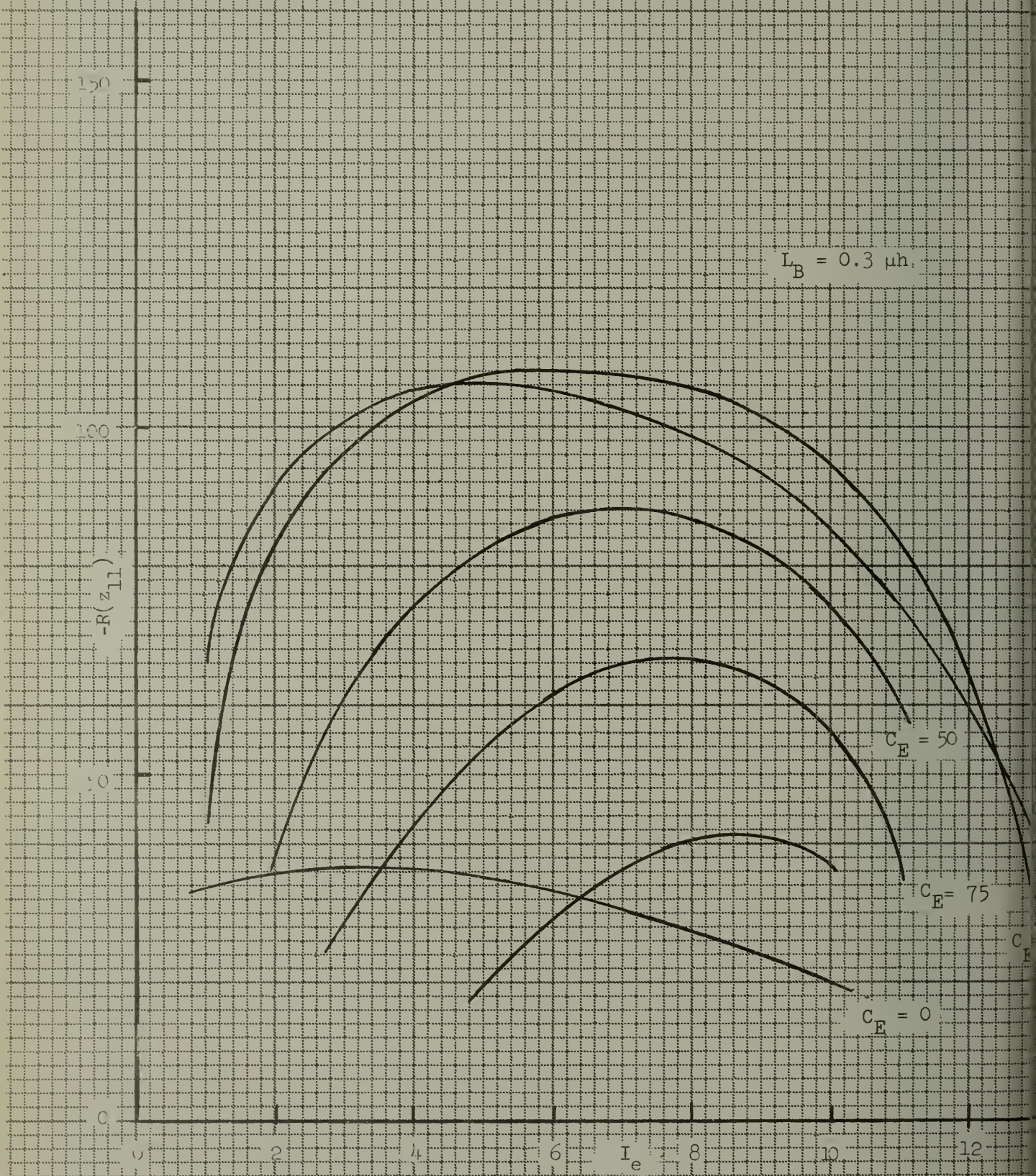


Figure 39

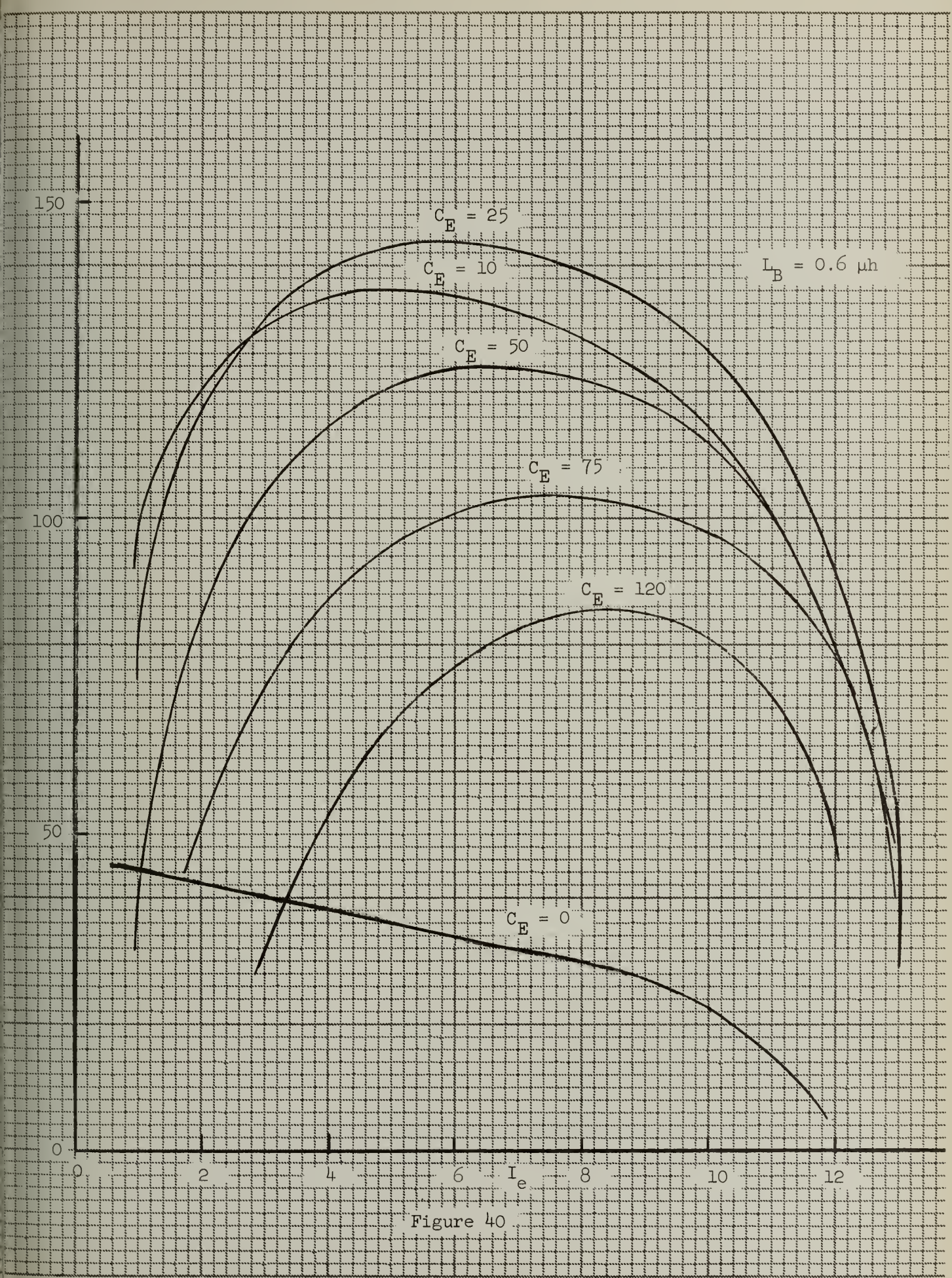

150
100
50
0
C_E = 25
C_E = 10
C_E = 50
C_E = 75
C_E = 120
C_E = 0
L_B = 0.6 μh
0
2
4
6
I_e
8
10
12

Figure 40

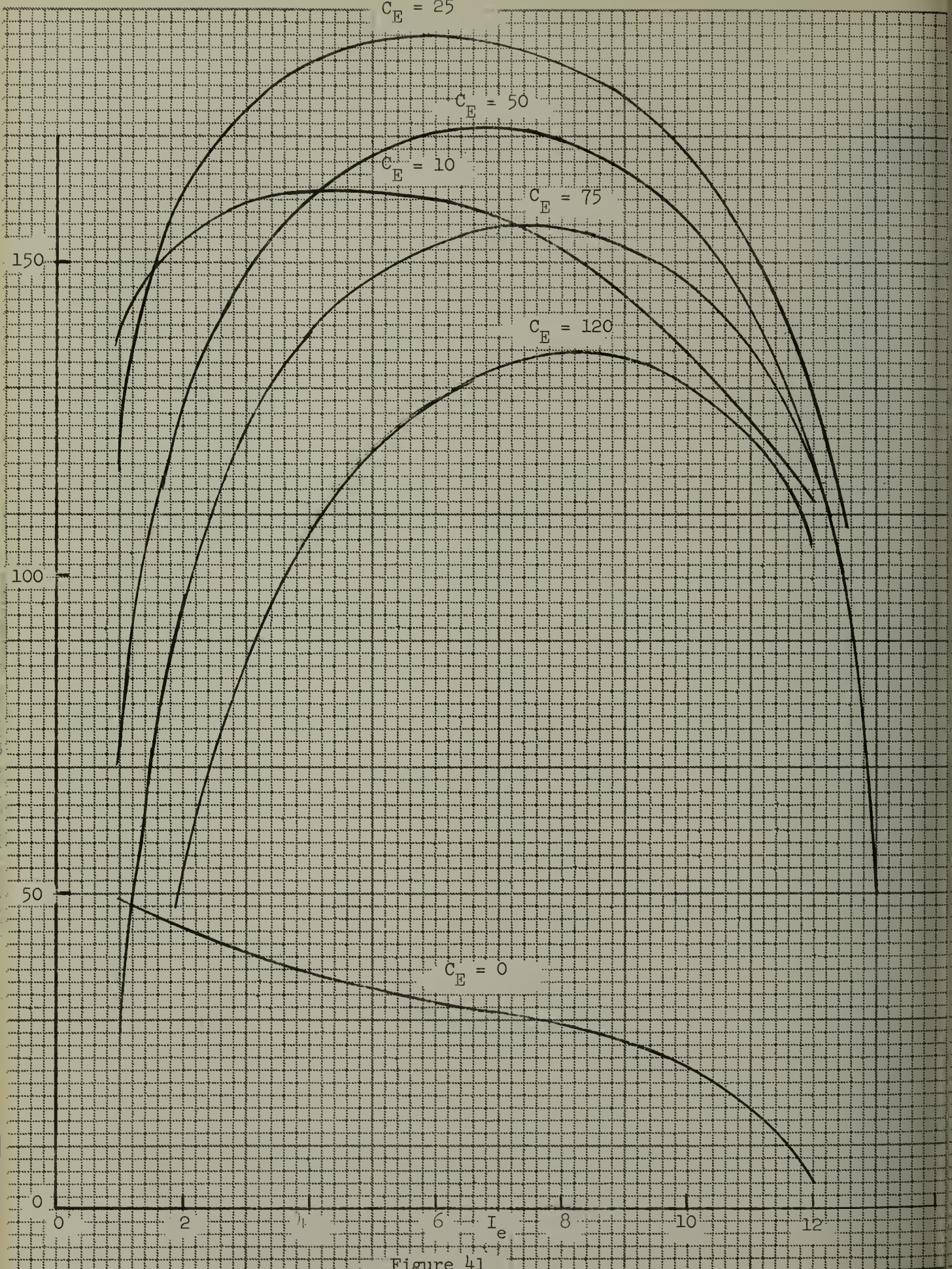


Figure 41

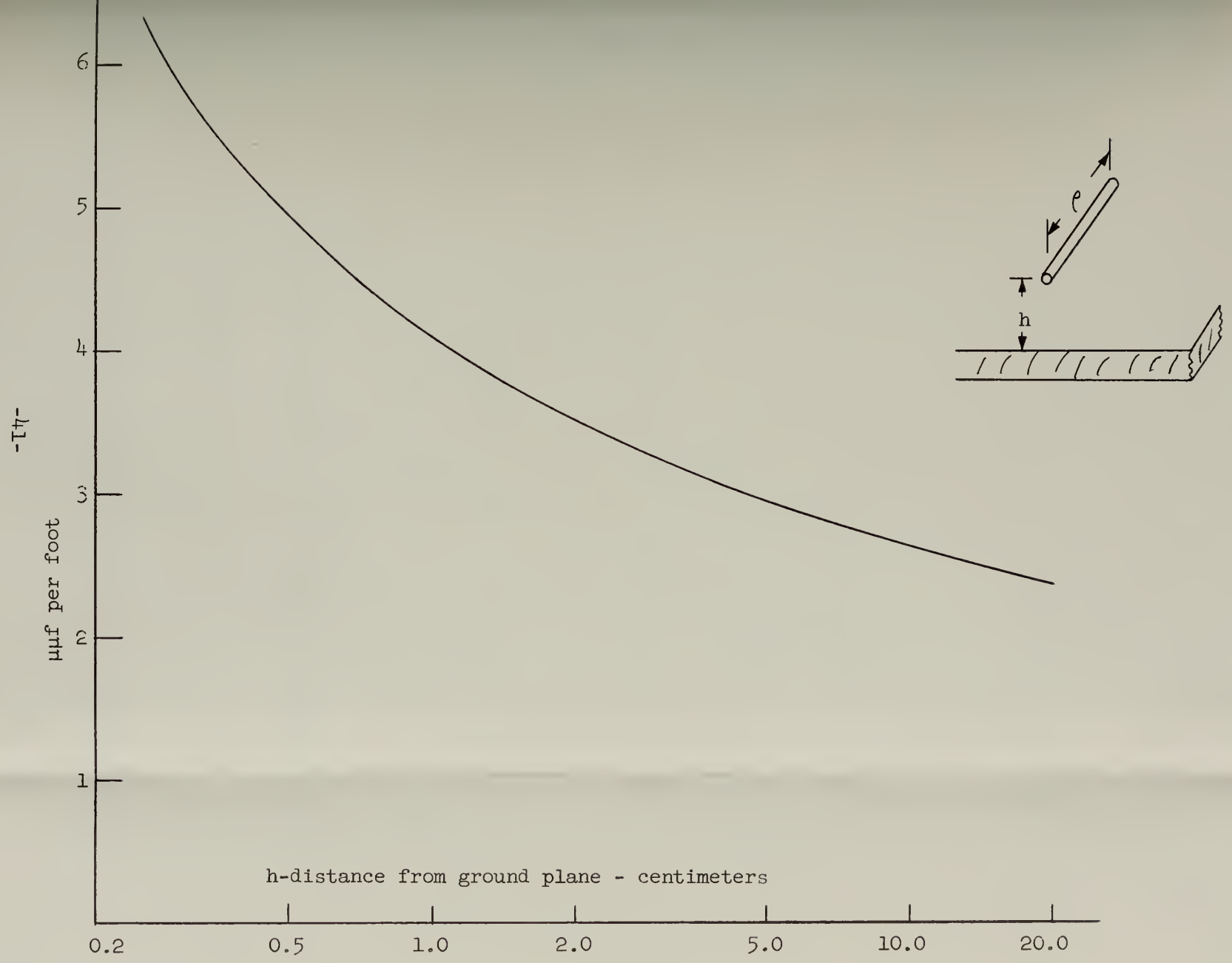


Figure 42

Wire to Ground Capacitance of a #22 Gage
Conductor above a Ground Plane

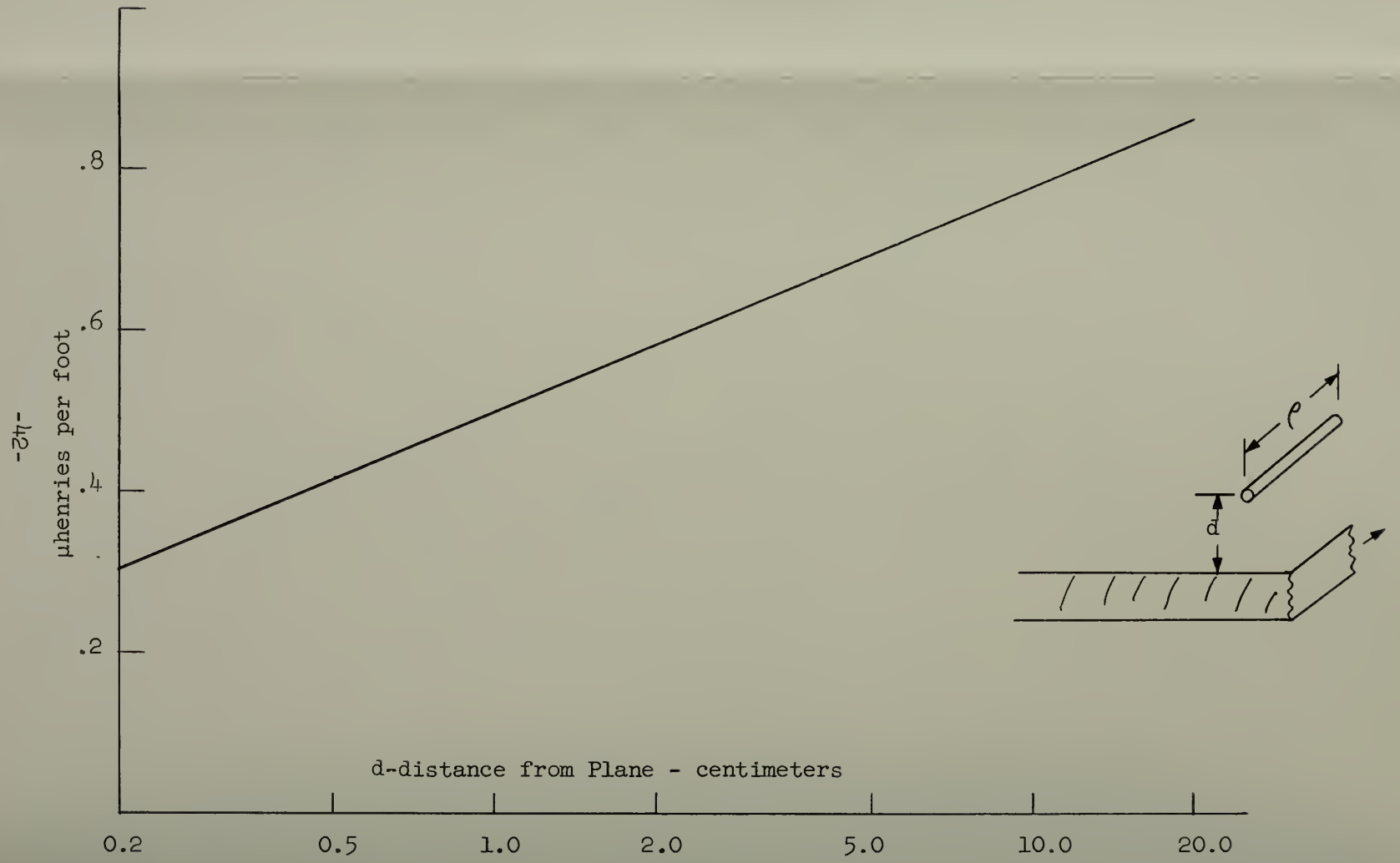


Figure 43

Self-Inductance of a #22 Gage Conductor
above an Infinite Ground Plane

The obtained data is given in the preceding four graphs. In order to estimate the value of L_B reference may be made to the plot of L vs. spacing over a ground plane. C_E can be computed by considering the previously-derived input impedance and the graphical representation of the wiring capacitance. For a detailed linear analysis the reader is referred to File No. 313 of this Laboratory.

Initial Transient:

Saturation effects were observed due to large feed-through effects In order to estimate their magnitude and cause, the following analysis is presented:

a) Base Drive:

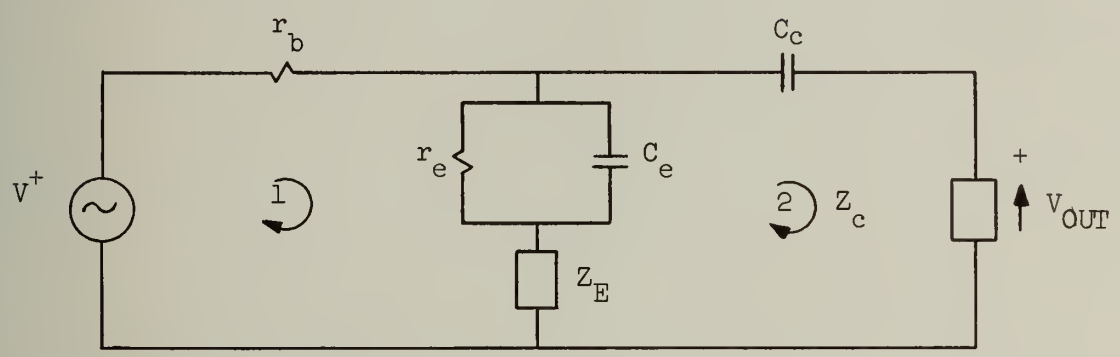


Figure 44

$$\begin{vmatrix} V \\ 0 \end{vmatrix} = \begin{vmatrix} r_b + Z_e + Z_E & -(Z_e + Z_E) \\ -(Z_e + Z_E) & (Z_e + Z_E + Z_c + \frac{1}{sC_c} \end{vmatrix} |i_1, i_2|$$

$$I_2 = \frac{Z_e + Z_E}{r_b(Z_c + 1/sC_c) + (Z_e + Z_E)(r_b + Z_c + 1/sC_c)} V$$

For most cases: $r_e \ll R_E$

$C_e \gg C_E$

and for capacitive loads:

$$V_2 = \frac{V}{(1 + \frac{r_b}{Z_E})(1 + \frac{1}{sC_cZ_c}) + \frac{r_b}{Z_c}}$$

if

$$V(s) = \frac{V_0}{s} \quad .$$

$$V_2 = \frac{V_0}{s^2 r_b(C_0 + aC_E) + s(ab + \frac{r_b}{R_c} + \frac{r_b C_E}{R_c C_c})} + \frac{b}{R_c C_c}$$

where

$$a = 1 + \frac{C_0}{C_c}$$

$$b = 1 + \frac{r_b}{R_E}$$

$$c = 1 + \frac{C_E}{C_c} \quad .$$

The roots of the denominator polynomial are given by:

$$s = -x \pm y \qquad x > y$$

$$x = \frac{ab + c\frac{r_b}{R_c}}{2r_b(C_0 + aC_E)}$$

$$y = \frac{1}{2r_b(C_0 + aC_E)} \sqrt{(ab + c\frac{r_b}{R_c})^2 - \frac{4br_b(C_0 + aC_E)}{R_c C_c}}$$

The normalized output is:

$$\frac{V_2}{V_0} = \frac{\epsilon^{-xt}}{r_b(C_0 + aC_E)y} \sinh |yt|$$

$$= \left[(ab + c\frac{r_b}{R_c})^2 - \frac{4br_b(C_0 + aC_E)}{R_cC_c} \right]^{-1/2} \left(\epsilon^{-(x-y)t} - \epsilon^{-(x+y)t} \right) .$$

The maximum with respect to time occurs when:

$$t = t' = \frac{1}{2y} \ln \frac{x + y}{x - y}$$

$$V_2(t') = \frac{V_0}{yr_b(C_0 + aC_E)} \left[\left(\frac{x - y}{x + y} \right)^{x/2y} \sinh \ln \left(\frac{x + y}{x - y} \right)^{1/2} \right] .$$

In order to minimize the output voltage, the only plysically realizable condition is given by:

$$x \gg y$$

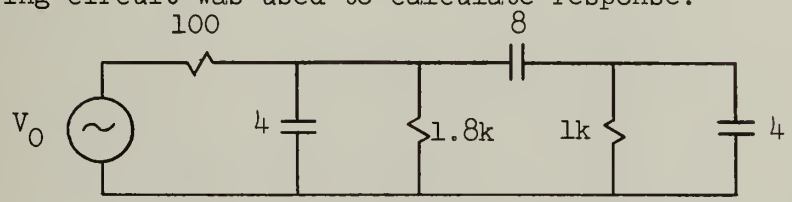
$$\frac{r_b}{R_cC_c} (1 + \frac{r_b}{R_E})(C_0 + C_E(1 + \frac{C_0}{C_c})) \gg 0 .$$

The minimum requires:

C_0, C_E, r_b are large,

C_c, R_E, R_c are small .

The following circuit was used to calculate response:



$$\frac{V_2}{V_0} = .672(\epsilon^{-0.08t} - \epsilon^{-1.57\epsilon}) \quad \text{(t in nanosceonds)}$$

Figure 45

Suppose now that r_b' is neglected. Then the output is given by:

$$V_2 = \frac{V_0}{as + \frac{1}{R_c C_c}}$$

$$\frac{V_2}{V_0} = \frac{1/a}{s + \frac{1}{aR_c C_c}}$$

$$\frac{V_2}{V_0} = \frac{1}{a} \epsilon^{-(t/aR_c C_c)}$$

$$\frac{V_2}{V_0} = \frac{C_c}{C_c + C_0} \epsilon^{-[t/C_0+C_c)R_c]}$$

For the equivalent circuit shown:

$$\frac{V_2}{V_0} = \frac{2}{3} \epsilon^{-t/12)} \quad .$$

The error is obvious. It is to be noted that this error becomes very small after the maximum of the exact waveform has been passed. This point is given by:

$$t' = \frac{1}{2y} \ln \frac{x + y}{x - y} \quad .$$

It is then approximately true that

$$\frac{V_2}{V_0} = \frac{C_c}{C_c + C_0} \epsilon^{[-1/R_c(C_0+C_c)]} (t + t') \quad .$$

The voltage across the depletion layer capacitance is

$$\frac{V_c}{V_0} = 1 - \frac{C_c}{C_c + C_0} \epsilon^{-[(t'+t)/R_c(C_0+C_c)]} \quad .$$

The conclusions are as follows:

1. The passive feedthrough is not negligible. About 50% of the input pulse appears at the collector output without phase inversion. The differentiated pulse is delayed by an effective t'.

2. The collector depletion layer capacitance is reverse polarized. The active current generator will have to remove this charge. This means that an effective pulse delay must result.

3. Passive feedthrough occurs for both current and voltage switching. It is thus unavoidable.

b) Emitter Injection:

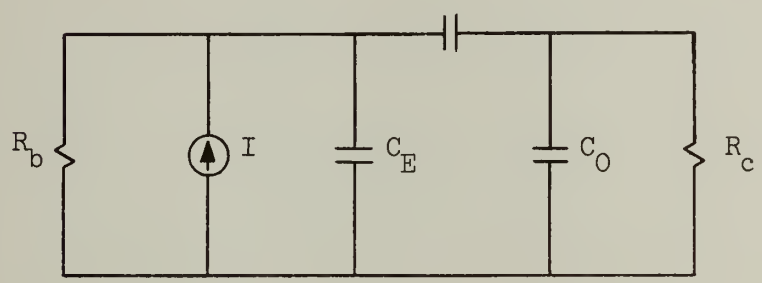


Figure 46

A formal solution is not necessary. By using the previous situation with the following conditions:

$$I_O = \frac{V_O}{R_b}$$

$$R_E \quad \infty \quad ,$$

the desired expressions may be obtained directly.

Pulse Feed-through
N-100 Passive Equiv.

Figure 47

$$\frac{V_2}{I_0} = \frac{\epsilon^{-xt}}{C_0 + aC_E} \sinh yt$$

$$x = \frac{\frac{a}{R_b} + \frac{c}{R_b}}{2(aC_E + C_0)}$$

$$y = \sqrt{(a + c\frac{R_b}{R_c})^2 - \frac{4R_b(C_0 + aC_E)}{R_c C_c}}$$

The time constants are equal if $r_b \ll R_E$. Identical response occurs if $I_0 R_b = V_0$. For the numerical example given, this means that unity base voltage swing corresponds roughly to an equivalent emitter current swing of 10 ma.

II. STORAGE ELEMENT

A. Flowflop: Boundary and Optimizing Conditions

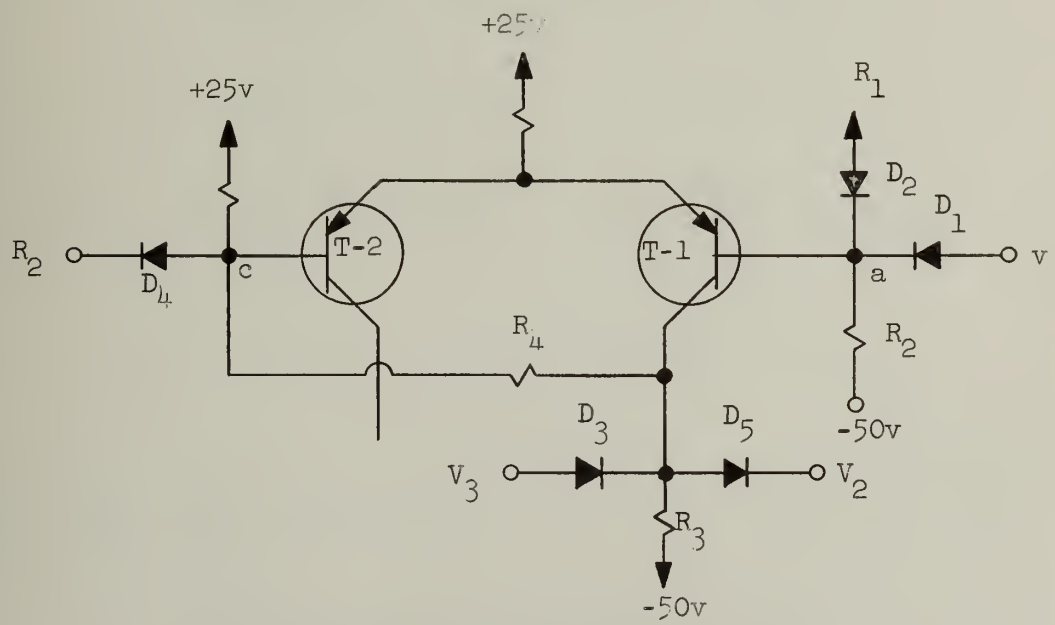


Figure 48

Notation: 1. Internal nodes are specified by small letters. The node letter is used as the first subscript on the variables.

2. The existence of a one or zero is designated by the corresponding subscript.

3. The store condition is noted by the prescript s.

4. Upper and lower band values are marked by bars above and below the variables.

5. The subscripts (1) and (2) refer to T_1 and T_2.

Switching speed analysis and tests on the N100 indicate that for optimum speed, a saturation margin of 2 volts with a collector current of approximately 15 ma is desirable.

Boundary conditions are considered in detail.

a) Gating Condition

For optimum design it is desirable to have the average potential at node c at the center of the gate-in band.

$$\frac{\bar{V}_c + \underline{V}_c}{2} = \frac{1}{2}\left(\frac{\bar{V}_{a1} + \underline{V}_{a1}}{2} + \frac{\bar{V}_{a0} + \underline{V}_{a0}}{2}\right)$$

$$\bar{V}_c = \bar{V}_{R2} + \bar{V}_{D4} \qquad \bar{V}_{a0} = \bar{v}_0 - \underline{V}_{D1(0)}$$

$$\underline{V}_c = \underline{V}_{R2} + \underline{V}_{D4} \qquad \underline{V}_{a0} = \underline{v}_0 - \bar{V}_{D1(0)}$$

$$\bar{V}_{a1} = v_1 - \bar{V}_{D1(1)}$$

$$\underline{V}_{a1} = \underline{v}_1 - \underline{V}_{D1(1)}$$

Substitution yields:

$$\frac{\bar{V}_{R2} + \underline{V}_{R2}}{2} + \frac{\bar{V}_{D4} + \underline{V}_{D4}}{2} = \frac{1}{2}\left[\frac{\bar{v}_1 + \underline{v}_1}{2} + \frac{\bar{v}_0 + \underline{v}_0}{2} - \frac{\bar{V}_{D1} + \underline{V}_{D1}}{2} - \frac{\bar{V}_{D0} + \underline{V}_{D0}}{2}\right]. \quad (8)$$

Equation (8) is an optimizing condition for the variables VR_2, v_1 and v_0. However, both variables contain additional constraints.

In order to ensure gating it is necessary that

$$\underline{V}_{a1} > \bar{V}_c \qquad (T\text{-}1 \text{ OFF})$$

$$V_{a0} < \underline{V}_c \qquad (T_1 \text{ ON})$$

An equality is not sufficient at this point. In the steady state, the circuit must act such that either of the two transistors are on, but not both. This requires that

$$\underline{V}_{a1} \geq \bar{V}_c + \bar{V}_{EB(2)} \qquad (T_2 \text{ ON})$$

$$\bar{V}_{EB(1)} + \bar{V}_{a0} \leq V_c \qquad (T_1 \text{ ON}) \ ,$$

which gives

$$\bar{V}_{R2} \leq \underline{v}_1 - \bar{V}_{D1(1)} - \bar{V}_{EB(2)} - \bar{V}_{D4} \qquad (9)$$

$$\underline{V}_{R2} \geq \bar{v}_0 - \underline{V}_{D1(0)} + \bar{V}_{EB(1)} - \underline{V}_{D4} \ . \qquad (10)$$

Equations (9) and (10) may be used to estimate the necessary band separation of the input signal. For typical values of the S577G diode and the N-100 transistor, voltage drops at 15 ma, (9) and (3) become

$$\bar{V}_{R2} = v_1 - 1.7$$

$$\underline{V}_{R2} = v_0 - .35 \ .$$

For a reasonable value of $\bar{V}_{R2} - \underline{V}_{R2}$, we use 1.2v (This boundary condition is discussed later.). Then

$$\Delta V_{R2} = 1.2 = v_1 - v_0 - 1.35$$

$$\Delta v = 2.6 \text{ volts.}$$

This means that a signal-free band approximately 3 volts wide must exist between a one and a zero input.

b) Input Circuit

The impedance level of the input circuit is set by the amount of base current required. Overcurrent should equal this value.

$$I_E(1 - \alpha) \leq 2I_b$$

$$\frac{\overline{25} + \underline{V}_{a0} - V_{EB(1)}}{\underline{R}_1} (1 - \alpha) \leq 2 \frac{\underline{50} - \underline{V}_{a0}}{\overline{R}_2}$$

$$\overline{R}_2 \leq 2\underline{R}_1 \frac{50 - (\underline{v}_0 - \overline{V}_{D1})}{(1 - \underline{\alpha})(\overline{25} + \underline{v}_0 - \overline{V}_{D1} - \underline{V}_{EB})} \quad . \tag{11}$$

c) Saturation Margin

During gating zero the base reaches its most negative value. The saturation margin, SM, should be specified at this point.

$$\underline{V}_{a0} - \overline{V}_{d0} = SM$$

$$SM \geq \underline{v}_0 - \underline{V}_2 - (\overline{V}_{D5} + \overline{V}_{D1}) \tag{12}$$

d) Power Dissipation

Maximum power dissipation occurs in T-1. The condition is given by

$$P_{Max} = \left(\frac{\overline{25} + \underline{V}_{D2} - \overline{V}_{R1} - \underline{V}_{EB(1)}}{\underline{R}_1} \right) \left(\overline{V}_{R1} - \underline{V}_{D2} - \underline{V}_2 + \overline{V}_{D5} \right)$$

$$\underline{R}_1 = \frac{1}{P_{Max}} \left(\overline{25} + \underline{V}_{D2} - \overline{V}_{R1} - \underline{V}_{EB(1)} \right) \left(\overline{V}_{R1} - \underline{V}_{D2} - \underline{V}_2 + \overline{V}_{D5} \right). \tag{13}$$

Hence (13) gives the minimum value of R_1 permissable for a given P_{Max}.

e) Collector Current

The impedance level of the collector circuit is determined by the minimum collector current. The collector current magnitude is a function of the saturation margin, the maximum emitter current (power dissipation limitations) and the minimum α. For maximum switching speed, as stated

previously, it is desirable to have a saturation margin of 2 volts and a collector current of approximately 15 ma. The minimum collector current is given by

$$i_{c_{Min}} = \underline{\alpha} \left(\frac{\underline{25} - \overline{V}_{EB} - \overline{V}_{R1} + \underline{V}_{D2}}{\overline{R}_1} \right) \quad . \tag{14}$$

f) Minimum Gain Requirement

The minimum collector current (with T_1 ON) is related to the voltage change at node d between the zero and one states by

$$\overline{V}_2 + \overline{V}_{D5} - (\underline{V}_3 - \overline{V}_{D3}) \geq i_{c_{Min}} \left(\frac{\underline{R}_3(R_4 + R_5)}{\underline{R}_3 + \underline{R}_4 + \underline{R}_5} \right)$$

and from (14)

$$\overline{V}_2 - \underline{V}_3 + \overline{V}_{D3} + \overline{V}_{D5} \geq \underline{\alpha} \left(\frac{\underline{25} - \overline{V}_{EB} - \overline{V}_{R2} + \underline{V}_{D2}}{\overline{R}_1} \right) \left(\frac{R_3(R_4 + R_5)}{\underline{R}_3 + \underline{R}_4 + \underline{R}_5} \right). \tag{15}$$

Equation (15) relates α_{Min}, R_1 and the divider resistors.

g) T_2 Base Current Divider Pull-Up

In the discussion of the required band separation of the input, an estimate of the change in the voltage at node c during gating was made in the store state, with D_4 OFF, the impedance of the R_3, R_4, R_5 divider must be sufficiently low to accept the base current of T-2 without causing large level shifts. The effective voltage change of node c (in the store state) due to T-2 base current is ΔV_c.

$$\Delta \overline{V}_c = (1 - \underline{\alpha}) \frac{\overline{\underline{25}} + \underline{V}_{R2} + \underline{V}_{D4} - \underline{V}_{EB(2)}}{\underline{R}_1} \left(\frac{\overline{R}_4 \overline{R}_5}{\overline{R}_4 + \overline{R}_5} \right) . \tag{16}$$

$\Delta \overline{V}_c$ should be within the "dead band" at node c.

h) Stability in Storing States

The isolation signal is supplied by R1. R1 must insure that D_1 is off for both v_0 and v_1. In addition, R_1 must maintain V_a in the "dead band" region of the flowflop to insure state retention steady state-wise. Isolation is assured if

$$\underline{sV}_a \geq \overline{v}_1$$

$$\underline{sV}_a = \underline{V}_{R1} - \overline{V}_{D2}$$

$$\underline{V}_{R1} \geq \overline{v}_1 + \overline{V}_{D2} \tag{17}$$

State retention requires that

a) $$\overline{sV}_{b1} \leq sV_{a1}$$

b) $$\overline{sV}_{b0} \leq sV_{c0} \quad .$$

Therefore

$$\underline{V}_{R1} \geq \overline{v}_c + \overline{V}_{D2} + \frac{\overline{25R}_4 + (\overline{V}_2 + \overline{V}_{D5})\underline{R}_5}{\overline{R}_4 + \underline{R}_5} - \overline{V}_{EB(2)} \tag{18}$$

$$\overline{V}_{R1} \leq \overline{V}_{D2} + \underline{V}_{EB(1)} + \frac{\overline{25R}_4 + (\overline{V}_3 - \overline{V}_{D3})\overline{R}_5}{\underline{R}_4 + \underline{R}_5} \quad . \tag{19}$$

Equations (18) and (19) are based on collector bumping conditions.

$$\underline{I}_{R4} \geq \overline{I}_{R3} \qquad \text{(One State)}$$

$$\underline{I}_{R4} + \underline{i}_{c(2)} \geq \overline{I}_{R3} \qquad \text{(Zero State)}$$

$$\frac{25 - \underline{V}_3 + \overline{V}_{D3}}{\overline{R}_4 + \overline{R}_5} \geq \frac{\overline{V}_3 + \underline{V}_{D3} - 50}{\underline{R}_3} \tag{20}$$

$$\frac{\overline{25} - (\underline{V}_2 + \underline{V}_{D5})}{\overline{R}_5 + \overline{R}_4} \geq \frac{\underline{V}_2 + \underline{V}_{D5} - \overline{50}}{\underline{R}_3} \tag{21}$$

i) Equations (20) and (21) express the necessary dc bumping conditions. However, for optimum dynamic performance, the inequalities in (19) and (20) should be replaced by equalities. This would produce minimum time delay due to bumping diode recovery time.

In addition to the boundary conditions discussed so far, one must insure that, under all worst-case tolerance limits, the reverse ratings of the transtor, and the transistor power dissipation are not exceeded in any of the various states. In this circuit there are four distinct dc states, namely "Gate One", "Gate Zero", "Store One" and "Store Zero". The following equations express the worst-case conditions which are pertinent to the analysis.

State: Gate One or Store:

Maximum I_E(T-2),

$$\bar{I}_e = \frac{\overline{25} - \underline{V}_c - V_{EB(2)}}{R_1}$$

Maximum V_c,

$$\bar{V}_4 = \overline{25} - \underline{I}_{R5}\,\underline{R}_5$$

$$\bar{V}_4 = \bar{R}_4\bar{I}_{R4} + \bar{V}_d$$

$$\bar{V}_4 = \overline{25} - \underline{V}_{EB(2)} - \underline{I}_{R1}\underline{R}_1$$

Maximum V_d,

$$\bar{V}_d = \bar{V}_3 - \underline{V}_{D3}$$

$$\bar{V}_d = \underline{I}_{R3}\underline{R}_3 - \overline{50}$$

Maximum emitter voltage (T-2),

$$\bar{V}_1 = \overline{25} - \underline{I}_{R1}\underline{R}_1$$

$$\bar{V}_1 = \bar{V}_{EB(2)} + \bar{V}_c$$

Maximum I_{R4},

$$\bar{I}_{R4} = \frac{\bar{V}_c - \underline{V}_d}{\underline{R}_4}$$

Maximum I_{R5}

$$\bar{I}_{R5} = \frac{\overline{25} - \underline{V}_c}{\underline{R}_5}$$

Maximum I_{R3}

$$\bar{I}_{R3} = \frac{-\overline{50} - \underline{V}_c}{\underline{R}_3}$$

Maximum I_{D4}

$$\bar{I}_{D4} \text{ at } \bar{V}_{D4} = \bar{V}_c - \underline{V}_{R2} \qquad \bar{I}_{D4} = \bar{I}_{R5} + \bar{I}_{b(2)} - \underline{I}_{R4}$$

Maximum I_{D3}(V_3 Bump)

$$\bar{V}_{D3} = \bar{V}_3 - \underline{V}_d$$

$$\bar{I}_{D3} = \bar{I}_{R3} - \underline{I}_{R4}$$

$$\underline{I}_{R4} = \underline{I}_{R5} + \underline{I}_{b(2)} - \bar{I}_{D4}$$

State: Gate Zero or Store Zero

Maximum emitter current (T_1)

$$\bar{I}_{E(1)} = \frac{\overline{25} - V_{EB(1)} - V_a}{\underline{R}_1}$$

$$\underline{V}_a = \underline{v}_1 - \bar{V}_{D1}$$

$$\underline{V}_a = \underline{I}_{R2}\underline{R}_2 - \overline{50}$$

$$\underline{V}_a = \underline{V}_{R1} - \bar{V}_{D2}$$

$$I_{R2} = I_{E(1)}(1 - \alpha) + I_{D1} + I_{D2}$$

Maximum collector voltage,

$$\bar{V}_d = \bar{I}_{R3}\bar{R}_3 - \underline{50}$$

$$\bar{V}_d = \bar{V}_{d5} - \underline{5}$$

$$\bar{V}_d = \bar{V}_c - \underline{I}_{R4}\underline{R}_4$$

$$\underline{I}_{R4} = \underline{I}_{R5} + \underline{I}_{b(2)} - \bar{I}_{D4}$$

Maximum emitter voltage,

$$\bar{V}_b = \overline{25} - \underline{I}_{R1}\underline{R}_1$$

$$\bar{V}_b = \bar{V}_{EB(1)} + \bar{V}_a$$

Maximum base voltage (T_2),

$$\bar{V}_c = \bar{V}_{D4} + \bar{V}_{R2}$$

$$\bar{V}_c = \overline{25} - I_{R5}R_5$$

$$\bar{V}_c = \bar{I}_{R4}\bar{R}_4 + \bar{V}_d$$

$$\bar{I}_{R4} = \bar{I}_{R5} + \bar{I}_{b(2')} - \underline{I}_{D4}$$

Maximum base voltage (T_1),

$$\bar{V}_a = \bar{v}_1 - V_{D1}$$

$$\bar{V}_a = V_{R1} - V_{D2}$$

$$\bar{V}_a = \bar{I}_{R2}\bar{R}_2 - \underline{50}$$

$$\bar{I}_{R2} = \bar{I}_{e(1)}(\overline{1 - \alpha}) + I$$

$$\bar{V}_a = \overline{25} - \underline{V}_{EB(1)} - \underline{I}_{R1}\underline{R}_1$$

Maximum I_{R2},

$$\bar{I}_{R2} = \frac{\overline{50} + \bar{V}_a}{\underline{R}_2}$$

Maximum I_{D1},

$$I_{D1} \text{ at } \bar{V}_{D1} = \bar{v}_1 - \underline{V}_a$$

Maximum I_{R3},

$$\bar{I}_{R3} = \frac{50 - \underline{V}_d}{\underline{R}_3}$$

Maximum I_{D5},

$$I_{D5} \text{ at } \bar{V}_c + \bar{5}$$

Maximum I_{R4},

$$\bar{I}_{R4} = \frac{\bar{V}_c - \underline{V}_d}{\underline{R}_4}$$

Maximum I_{R5},

$$\underline{I}_{R5} = \frac{\overline{25} - \underline{V}_c}{\underline{R}_5}$$

Maximum I_{D4}

$$I_{D4} \text{ at } \bar{V}_{D1} = \bar{V}_c - V_{R2}$$

B. Method of Design

This section is not intended to concern itself with basic design principles. It merely serves as an aid to a better understanding of the tolerance properties of the circuit. This limits the discussion to the collector circuit and the associated bleeder.

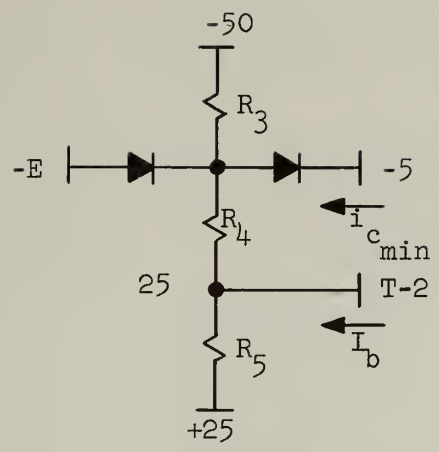


Figure 49

a) Maximum Expected Base Current: 1 ma

Maximum allowable pull-up: $\bar{v}_p$

$$\frac{R_4 R_5}{R_4 + R_5} \; 1.03 \leq \bar{v}_p$$

$$R_4 \leq \frac{R_5 \bar{v}_p}{1.03R_5 - \bar{v}_p}$$

This equation is evaluated on the design plot for $\bar{v}_p = 0.5v$ (Figure 50.2), $\bar{v}_p = 1.0v$ (Figure 50.1), and $\bar{v}_p = 1.5v$ (Figure 50.3).

b) T-2 "Off"

$$v_{Min} \geq 5.0v$$

$$\bar{v} \geq 24.25 \frac{R_4 \cdot .97}{97R_4 + 1.03R_5} - 5.0 \frac{1.03R_5}{1.03R_5 + .97R_4}$$

$$R_4 + R_5 \leq 1.55R_5 \qquad \text{(Figure 50.4)}$$

c) T-2 "Off"

$$v_{max} \leq 8.5v$$

$$v_{Max} \leq 25.75 \frac{R_4 \cdot 1.03}{.97R_5 + 1.03R_4} - 4.2 \frac{.97R_5}{.97R_5 + 1.03R_4}$$

$$R_4 + R_5 \geq 1.694R_5 \qquad \text{(Figure 50.5)}$$

d) Minimum Gain Requirement:

1. $$\frac{50 - 5}{R_3} < i_c + \frac{25 + 5}{R_4 + R_5}$$

$$R_3 > \frac{50 - 5}{i_c + \frac{25 + 5}{R_4 + R_5}}$$

$$R_3 \geq \frac{47.3}{i_{c_{Min}} + \frac{27.6}{R_4 + R_5}}$$

This curve was evaluated for $i_{c_{Min}} = 10$ ma. (Figure 50.6)

2. $$\frac{50 - 13.5}{R_3} > \frac{25 + 13.5}{R_4 + R_5}$$

$$R_3 \leq .814(R_4 + R_5) \qquad \text{(Figure 50.7)}$$

e) T-2 "On"

$$v_{Min} \geq -1.0$$

$$25 \frac{R_4}{R_5 + R_4} - E \frac{R_5}{R_4 + R_5} \geq -1.0$$

1. $$R_4 \geq \frac{(1.0E - 1.61)R_5}{26.4}$$

T-2 "On" - $v_{Max} \leq 1.5$

$$25 \frac{R_4}{R_5 + R_4} - E \frac{R_5}{R_4 + R_5} \leq 1.5$$

2. $$R_4 \leq \frac{(.94V_3 + 1.35)R_5}{25.05}$$

The minimum value for V_3 is given by:

$$\frac{.94V_3 + 1.35}{25.05} = \frac{1.06V_3 - 1.61}{24.4}$$

$$V_3 = 12.7 \text{ volts.}$$

In order to minimize the collector swing and thereby decrease the switching time V_3 should be as close as possible to this value.

For V_3 = 13.5v, the equations reduce to:

a) $R_4 \geq .52\ R_5$ (Figure 50.8)

b) $R_4 \leq .56\ R_5$ (Figure 50.9)

The solution from the graph yields the following set of values:

If $i_{c_{Min}} = 10$ ma

$R_3 = 2.7$ k	$R_3 = 2.7$ k
$R_4 = 1.3$ k	$R_4 = 1.2$ k
$R_5 = 2.3$ k	$R_5 = 2.2$ k

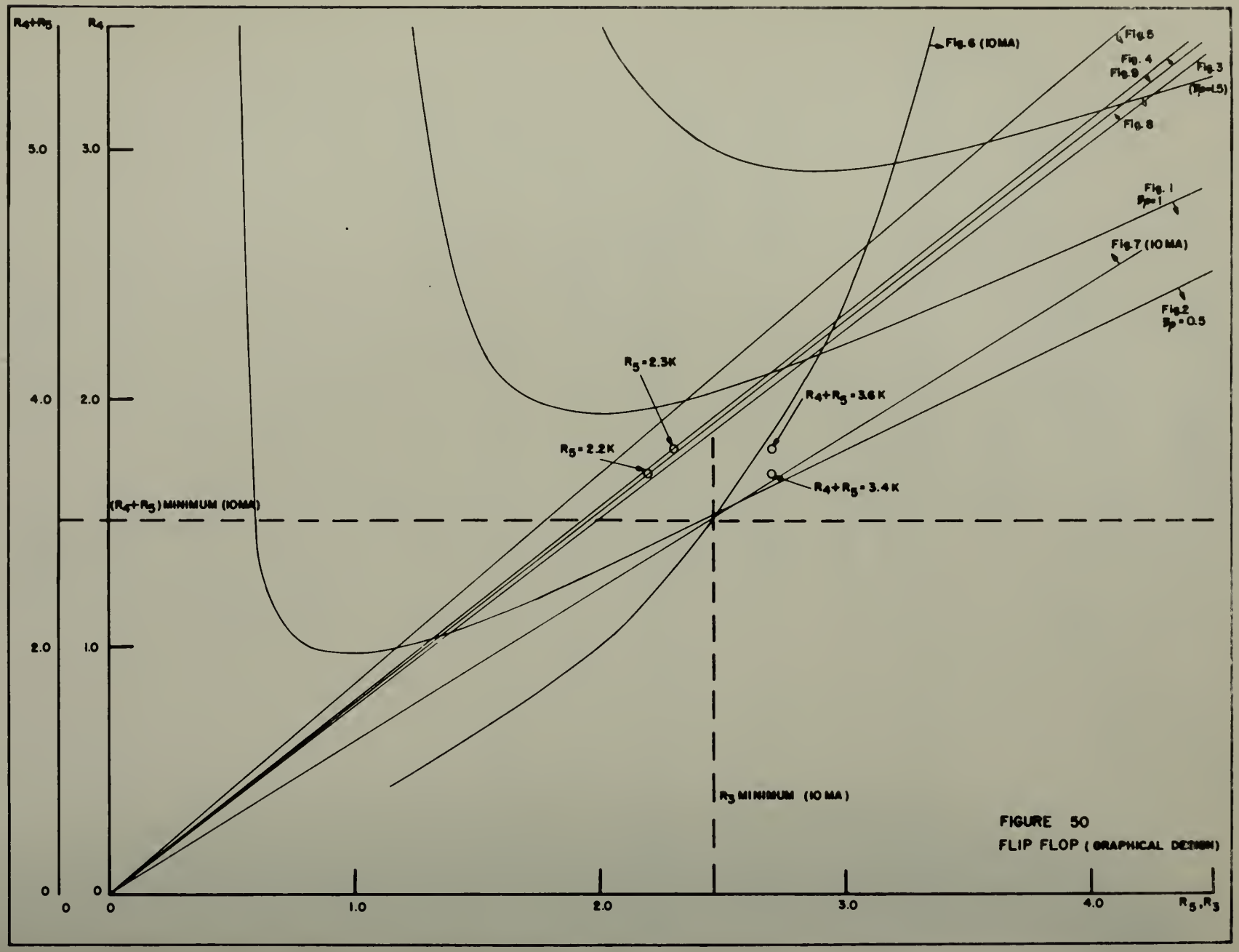


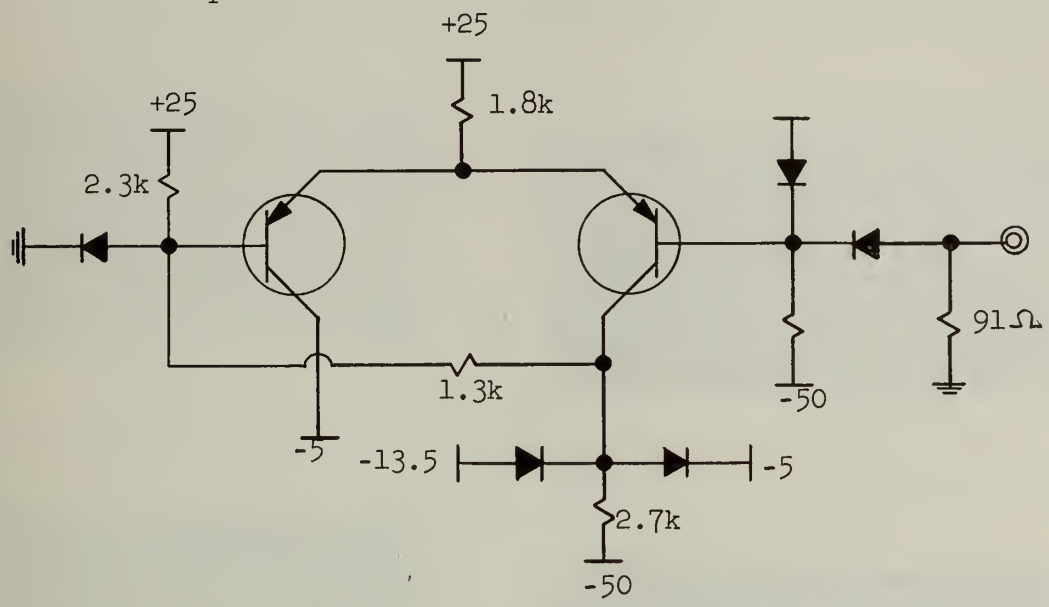
FIGURE 50
FLIP FLOP (GRAPHICAL DESIGN)

III. DESIGN EVALUATION

A. Flowflop

The design without output circuit was tested dynamically as a switching amplifier to study the effect of tolerance variations on speed. The test circuits are shown. Results are presented in the form of photographs and need no further comments.

Test circuit for input waveform:



All resistors variable 0%, ±3%; all power supplies variable.

Figure 51

Input current measurement:

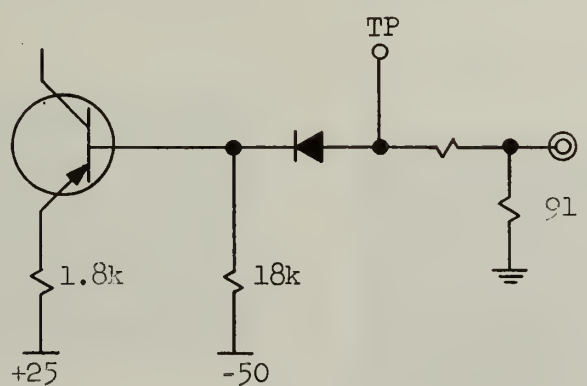


Figure 52

All traces 10 nsec/cm

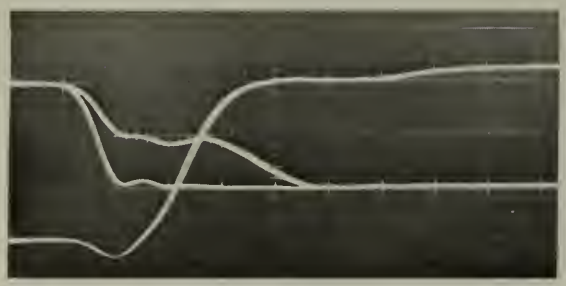
a) Input +1.5v
-1.5v 1v/cm

b) T-1 Base 1v/cm

c) T-1 Collector 2v/cm

Figure 53

Minimum Specified Input Signal (Nom.)



All traces 10 nsec/cm

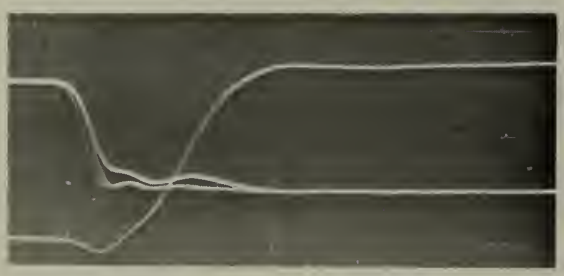
a) Input +1.5v
-2.5v 2v/cm

b) T-1 Base 2v/cm

c) T-1 Collector 2v/cm

Figure 54

Maximum Negative Input Signal (Nom.)



All traces 10 nsec/cm

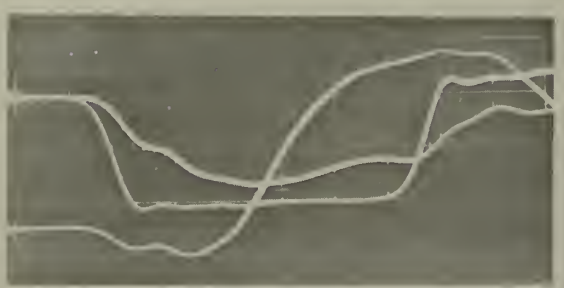
a) Input +1.5v
-0.5v 1v/cm

b) T-1 Base 1v/cm

c) T-1 Collector 2v/cm

Figure 55

Marginal Input Signal (Nom.)



All traces 10 nsec/cm

a) Input +1.5v 2v/cm

b) Generator Output 2v/cm

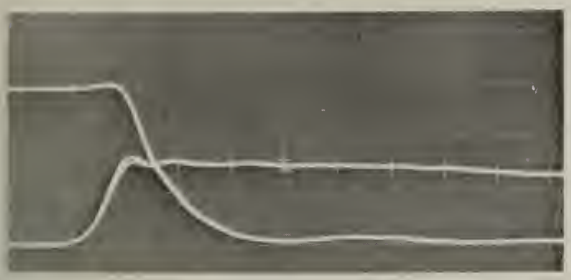
c) Collector 2v/cm

(Refer to Figure 52)

Figure 56

Transient Input Current
(Worst Case Tolerances)

Input Characteristics: Gate "1"



10 nsec/cm, 2v/cm

a) Collector T-1

b) Input -1.5v/+1.5v

c) Base T-1

Figure 57

Minimum Specified Positive Input (Nominal)

Scale: Same as Figure 57

a) Collector T-1

b) Input -1.5v/+3.2v

c) Base T-1

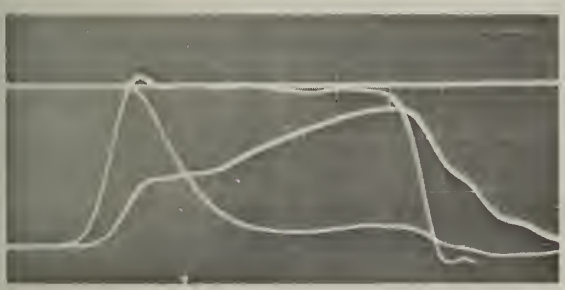
Figure 58

Maximum Specified Positive Input (Nominal)

Same as Figure 57

Figure 59

Marginal Input Signal (Nominal)



10 nsec/cm, 2v/cm

a) Generator Output

b) Input T-1

c) Collector T-1

Test Circuit Figure 52

Figure 60

Transient Input Current (Worst Case)

Speed Dependence on Tolerance Conditions:

a) Gate "1"

Figure 61

Worst Case
(Power Supplies, Resistors, Input)

Scale: 10 nsec/cm, 2v/cm

Condition:

+25+	2.7k+
-50-	1.3k-
-13.5+	18k+

Tolerances on Magnitude Input: +1.5v

a) Collector T-1

b) Input

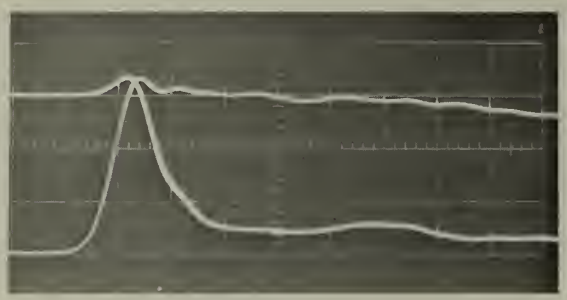


Figure 62

Best Case

See Figure 61

All tolerances reversed

b) Gate "0"

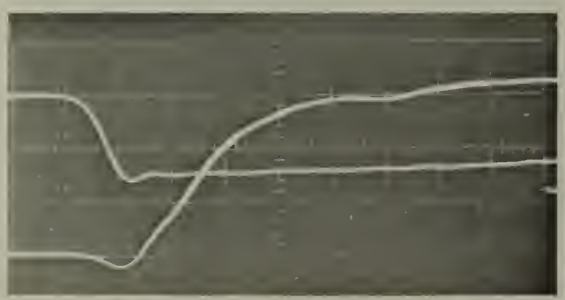


Figure 63

Worst Case

Condition:

-50+	2.7k-
- 5+	1.3k+
+25-	2.3k+
+13.5+	18k+

Input: $\pm$1.5v

Figure 64

Best Case

See Figure 63

All tolerances reversed

B. Average Tests

a) Free-running Flipflop Test

The following test circuit was used to obtain data on the average flipflop speed. The somewhat academic assumption of perfect drivers permits a flow-gating system which is limited only by the speed of the storage element. It is to be noted that interconnection between flipflops was not the same as that envisioned in the final system.

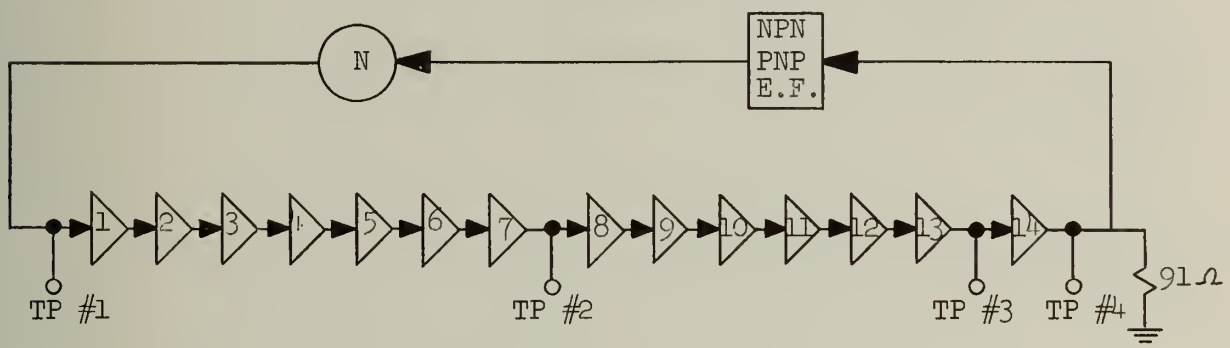


Figure 65

Free running speed:

In order to calculate expected asymmetric waveforms within the chain the following formulas are developed: (see next page)

The down-time for the m^{th} flipflop is given by:

$$t_D = \sum_{m+1}^{14} t_{f_i} + \sum_{1}^{m} t_{r_i} + t_{nl}$$

if

$$\bar{t}_f \equiv \frac{1}{14} \sum_{1}^{14} t_{f_i}$$

$$\bar{t}_r \equiv \frac{1}{14} \sum_{1}^{14} t_{r_i}$$

$$t_D \approx (14 - m)\,\bar{t}_f + m\bar{t}_r + t_{nl}$$

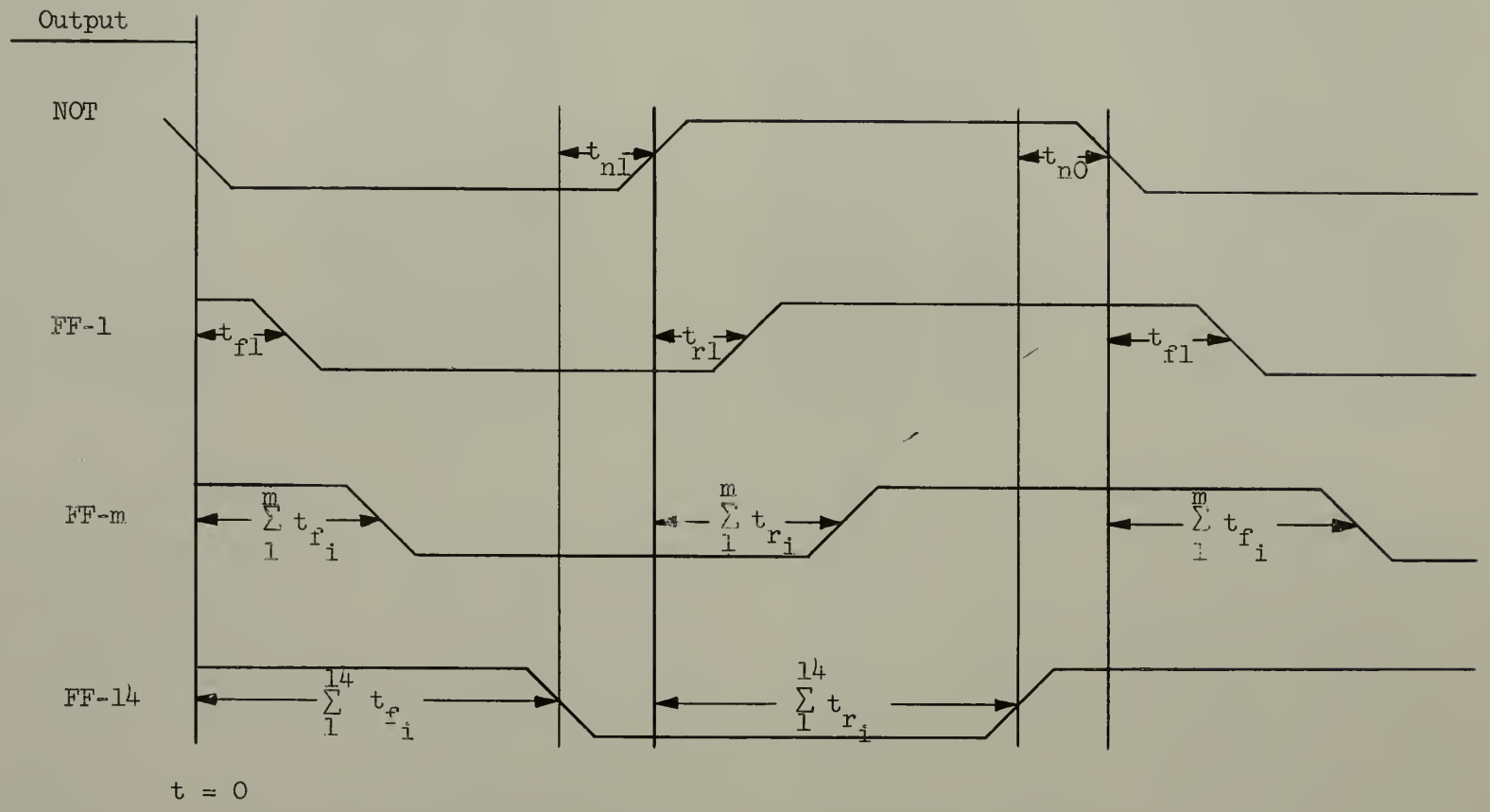

Output
NOT
FF-1
FF-m
FF-14
t_{n1}
t_{n0}
t_{f1}
t_{r1}
t_{f1}
$\sum_{1}^{m} t_{f_i}$
$\sum_{1}^{m} t_{r_i}$
$\sum_{1}^{m} t_{f_i}$
$\sum_{1}^{14} t_{f_i}$
$\sum_{1}^{14} t_{r_i}$
t = 0

Figure 66

Similarly:

$$t_u \approx (14 - m)\,\bar{t}_r + m\bar{t}_f + t_{n0}$$

where t_u is the up-time of the m^{th} flipflop. The cycle time, t_c is then

$$t_c \approx 14(\bar{t}_f + \bar{t}_r) + t_{n1} + t_{n0} \quad .$$

The symmetry condition $t_D = t_u$ is given by

$$m = \frac{n}{2} + \frac{t_{n0} - t_{n1}}{2(\bar{t}_r - \bar{t}_f)}$$

$$m \approx \frac{n}{2}$$

where n is the total number of identical elements.

Experimental data was taken to determine the four parameters involved in the above formulas. Waveforms were taken at the three points indicated. The basic speed of the system is approximately:

$$f = \frac{1}{\bar{t}_f + \bar{t}_D}$$

$$= \frac{10^9}{45.8}$$

$$f = 21.9 \text{ mc}$$

Experimental Data: Free-running flipflop

	t_f	t_r
1	32	18
2	29	16
3	30	12
4	30	18
5	28	14
6	34	11
7	26	16
8	28	16
9	30	18
10	32	16
11	28	14
12	30	14
13	28	28
14	29	16

$t_{n1} = 42$ nsec

$t_{n0} = 26$ nsec

$\bar{t}_f = 29.57$ nsec

$\bar{t}_r = 16.21$ nsec

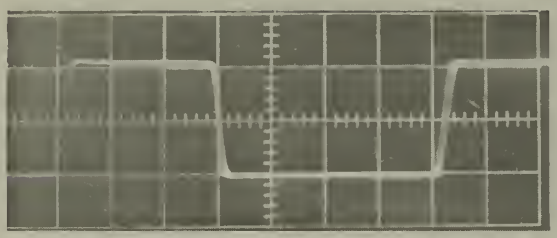


Figure 67

TP #1

Scale: 100 nsec/cm

2v/cm center ground

Calculated Values:

t_{u1} = 282 nsec

t_{D1} = 456 nsec

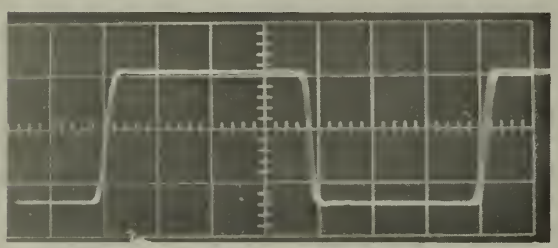


Figure 68

TP #2

Scale: Same as TP #2

Calculated Values:

t_{u7} = 362 nsec

t_{D7} = 346 nsec

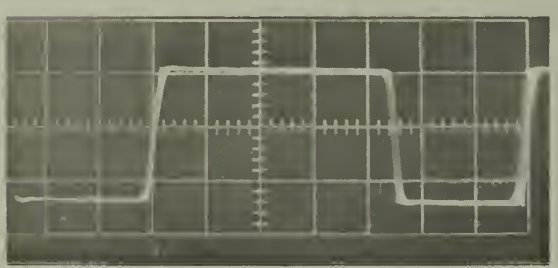


Figure 69

TP #3

Scale: Same as TP #3

Calculated Values:

t_{u13} = 427 nsec

t_{D13} = 280 nsec

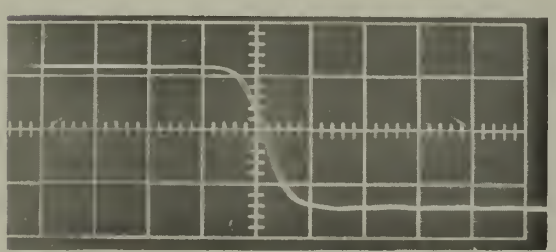
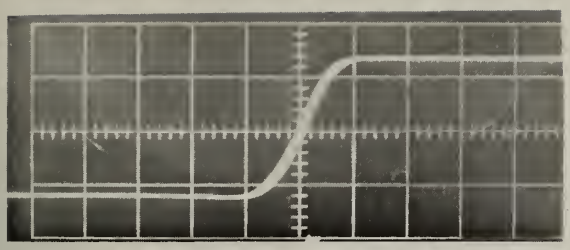


Figure 70

Scale: 20 nsec/cm

2v/cm 0 volt center

TP #2 Fall-time



Scale: 20 nsec/cm
2v/cm 0 volt center
TP #2 Rise-time

Figure 71

b) Free Ring Test

In order to test read-in driver and flipflops, the system shown was connected. Use is made of the natural delay of the flowflop. The resulting waveforms are shown.

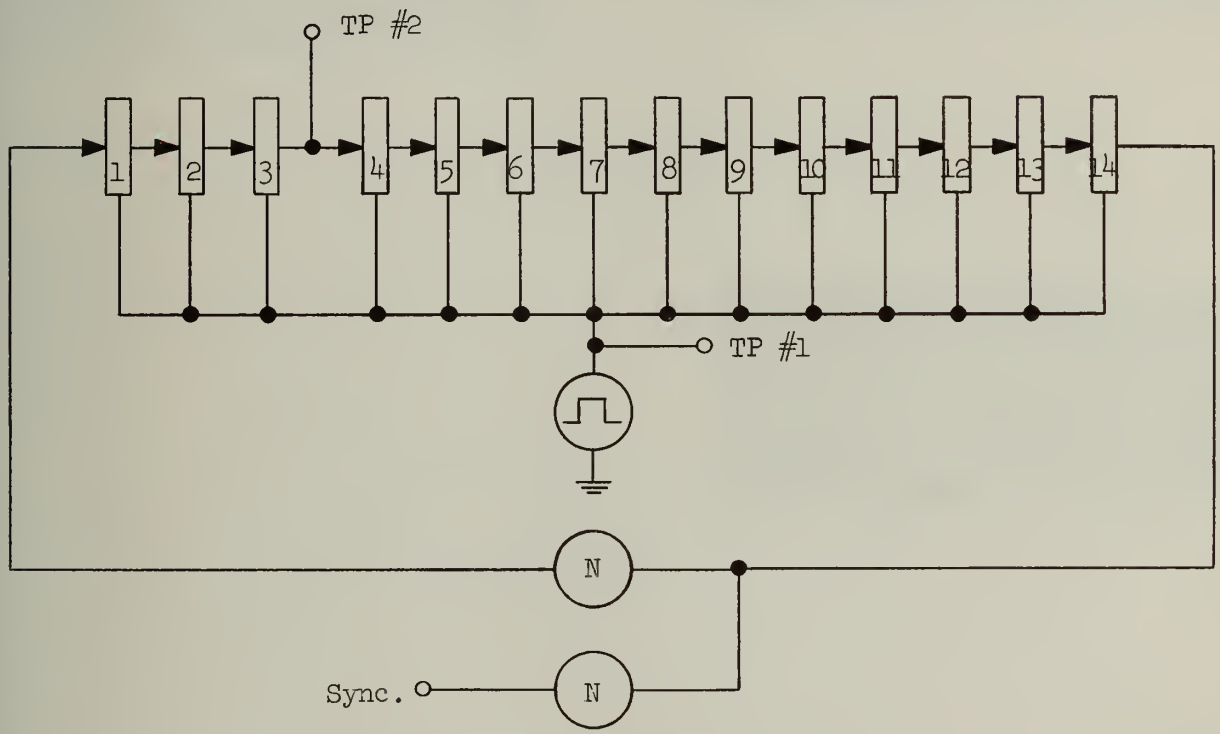
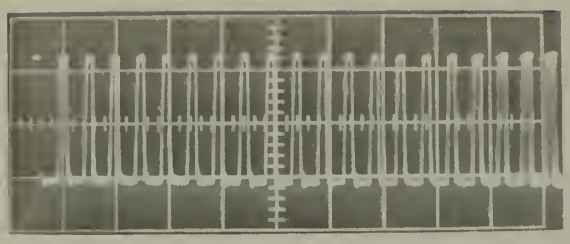
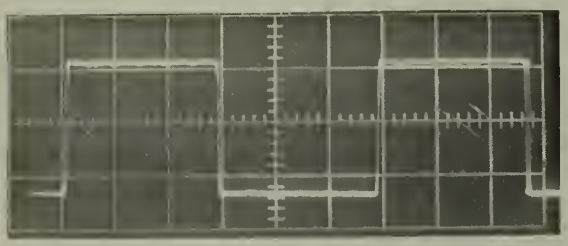


Figure 72



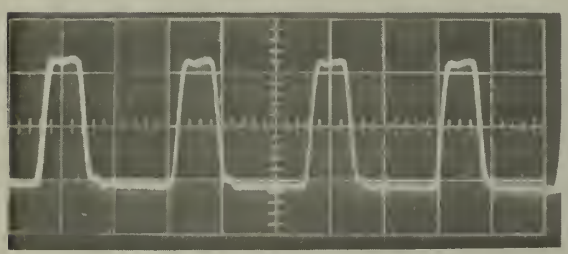
TP #1
Scale: 0.5 μsec/cm
2v/cm 0 volts at center

Figure 73



TP #2
Scale: Same as above
Division by seven

Figure 74



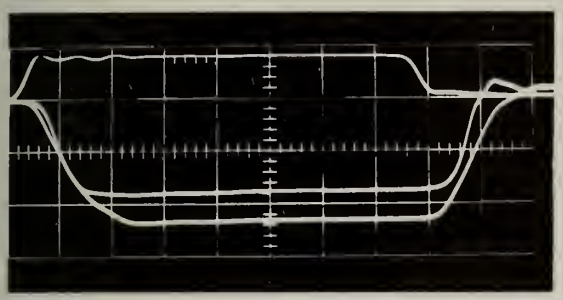
TP #1
Scale: 100 nsec/cm
2v/cm
Speed 4 mc

Figure 75

c) Read-in Driver

The proper design of the over-all system is connected closely to the balance in speed and other characteristics between the flipflop and read-in driver. Initial considerations of driver circuitry resulted in the choice of a low-power-transistor driver rather than the high-power-transistor version.

From the preceding sections it becomes obvious that the read-in driver must have two outputs, which differ in DC-level and AC-swing, but are in time phase. One of these outputs serves as the isolation signal to the input circuit of the storage element, while the other one disconnects the feedback loop to the Schmitt-Trigger. The necessary load currents for the two circuits differ considerably so that more power is required to operate the feedback circuit than the isolate circuit.



Scale: 4v/cm
20 nsec/cm

a) Input without Pre-driver

b) Isolate Output

c) Feedback Output

Figure 76

In order to increase the effective saturation margin of the flowflop, the isolator output was limited, so that it will in no case become more negative than 2.4 volts. This implies that gating into the device by input signals which are more negative than 2.4 volts is accomplished by the driver and not the actual input bus.

In order to minimize the oscillation possibility, it is strongly recommended that the negative bumping diodes on the bases of the feedback-control part of the driver be connected in such a way that they are physically located at the base of the N-100 which is furthest from the GF-45011 collector stage.

d) Output Circuits

As stated earlier, the basic idea of the output circuitry is that of a CURRENT-OR circuit, its inputs being the flowflop and the send-driver. Since PNP transistors are forced by compatibility and the CURRENT-OR is

proposed, the use of a collector as a current source suggests itself. This implies that it is easier to furnish a current source than a current sink. However, this is in the end beneficial as far as the magnitude of source or sinkcurrent is concerned.

An additional restriction is placed on the output circuit by its loading conditions. It is envisioned that an n input AND circuit was to be driven, where n is the number of registers in the block. The physical spacing is by necessity large, so that capacitive loading effects are high. Since the cost of the proposed transistor is comparable to that of a high-speed diode it is proposed to replace the diode by a transistor.

The resulting output circuit is as shown:

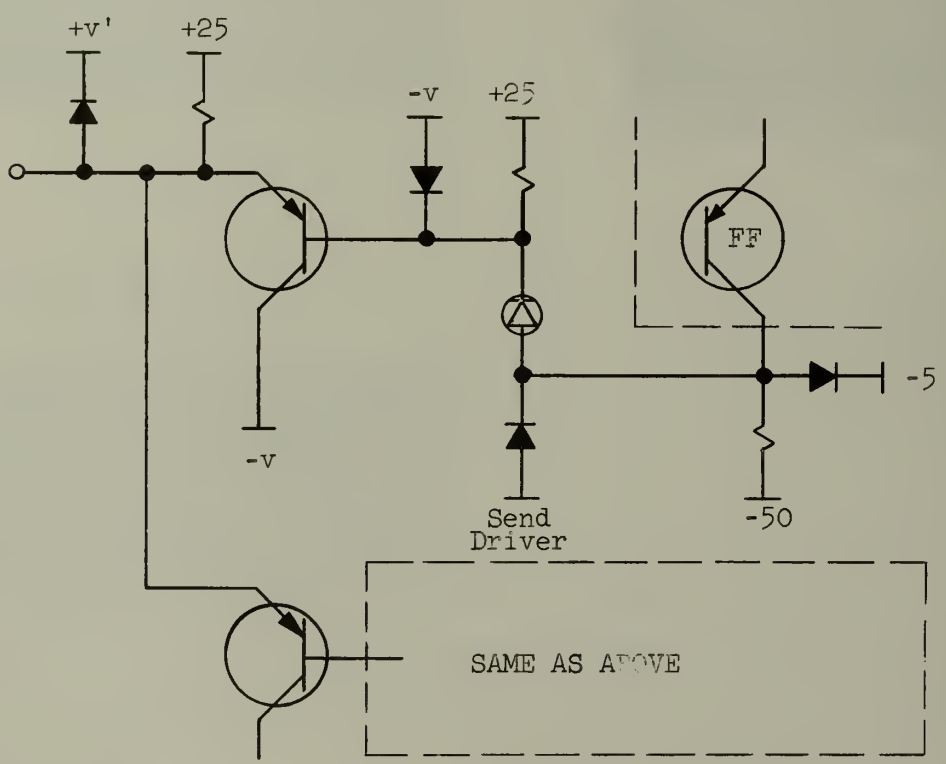


Figure 77

The send-driver follows directly from this circuitry. It employs in order a level-shifter, which is used to suppress emitter-follower oscillations, a buffer amplifier and a current switch. The emphasis on speed requires the use of a PNP-NPN emitter-follower as a buffer, which was the facility to provide overcurrent in both directions.

The result is then as follows:

1. Input to send-driver positive - output of AND circuit positive

2. Input to send-driver negative - stored information of flipflop at output of send-circuit.

The difficulties associated with the distributed AND circuit are partly eliminated if the following construction procedure is used.

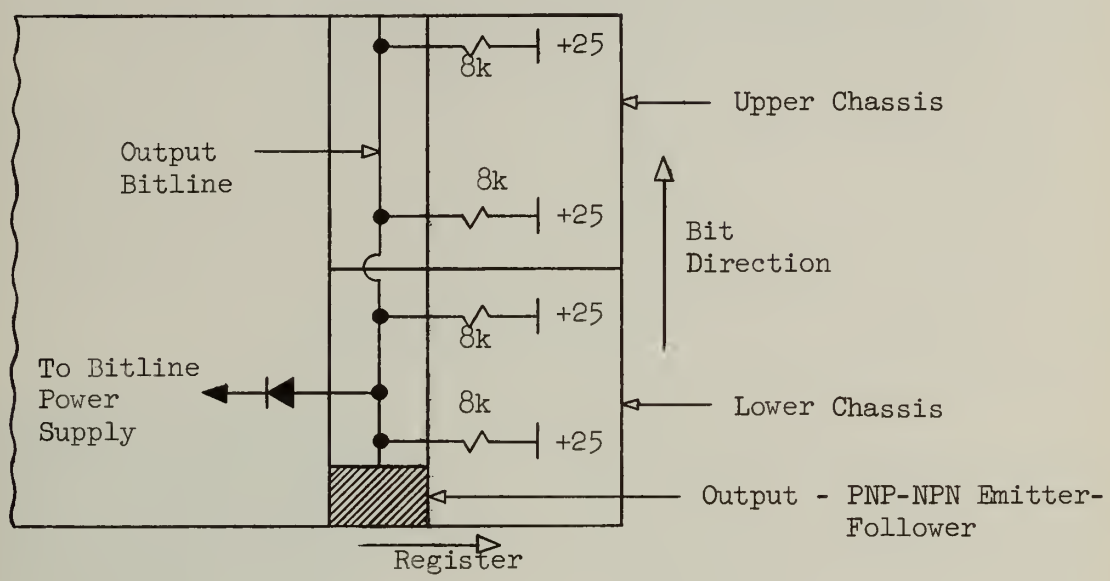
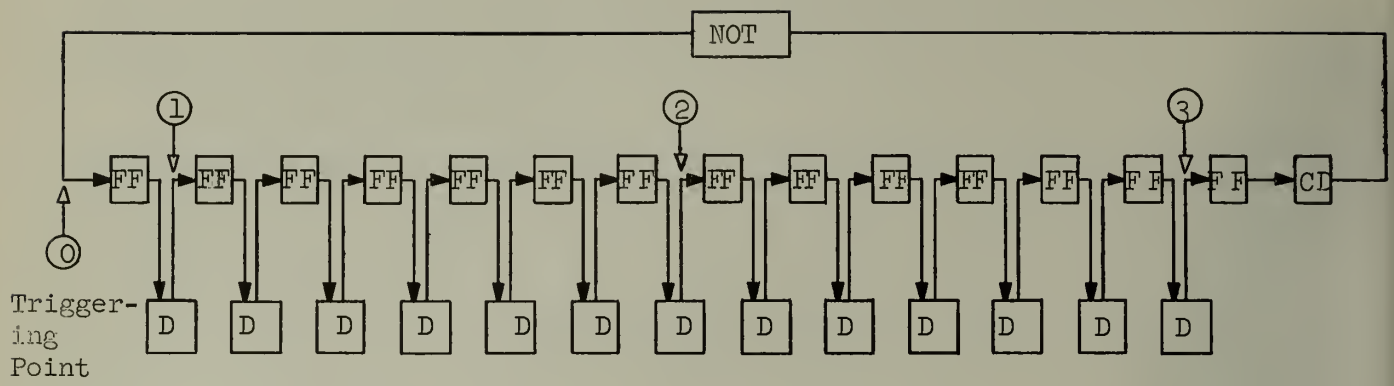


Figure 78

IV. SYSTEMS TESTS

A. Free-running Delay Calibration Test

In order to obtain information on read-in behavior additional delay within the flopflop eases the somewhat critical timing problem with respect to read-in driver pulse length. The arrangement shown in Figure 79 allows delay unit calibration. The delay circuit (Figure 81) will disturb the flowflop output emitter follower, but will not affect the storage action of the flowflop.



CD = cable driver
(N-100 - N-101
emitter-follower)

FF = flowflop

D = delay circuit

Figure 79

Free-running Register

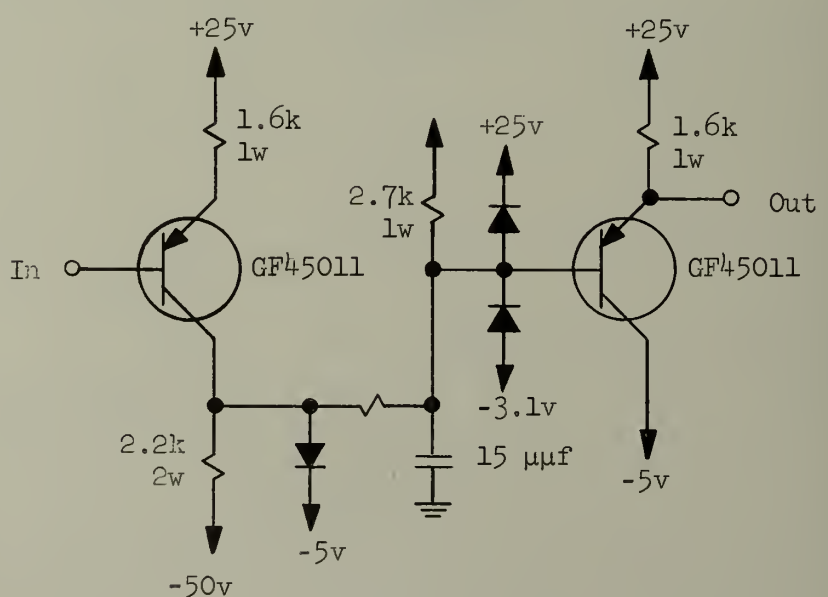


Figure 80

NOT Circuit

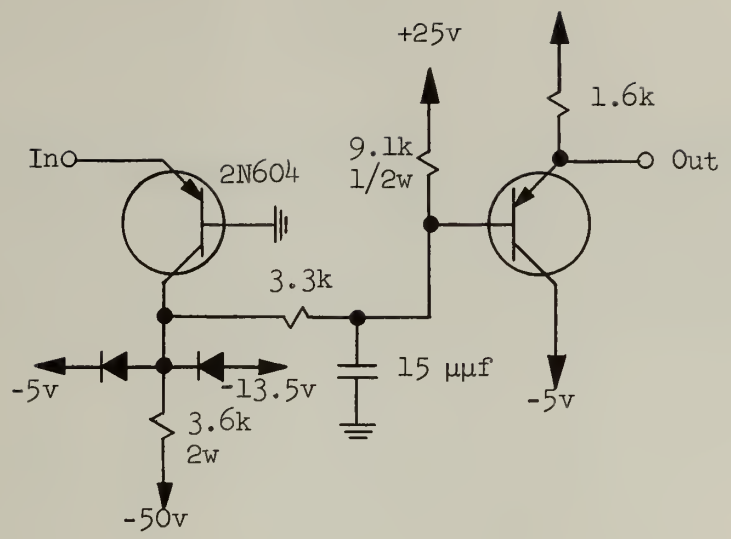
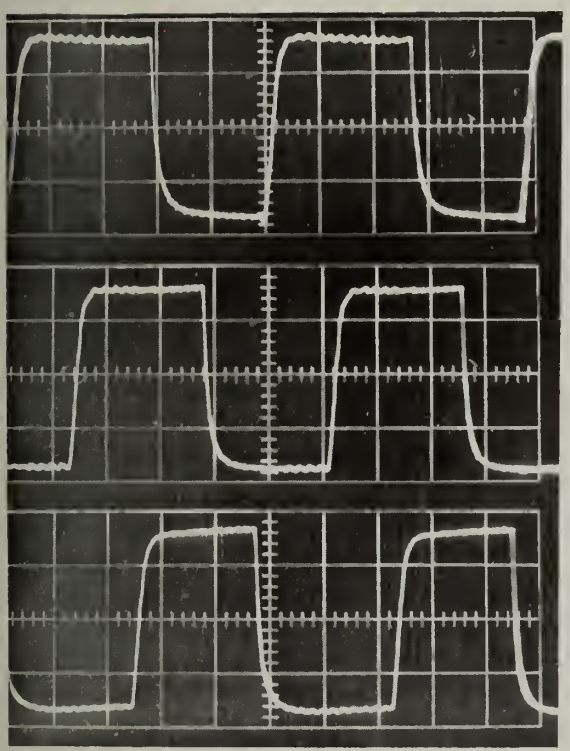


Figure 81

Delay Circuit



TP #1

TP #2

TP #3

The ripples are not oscillations but the induced noise caused by the propagation of wave fronts. The number of ripples is 14. The average delay time of the delay circuit is:

[(period with delays) - (period without delay)] ÷ 15 ÷ 2

= (2400 - 710) ÷ 15 ÷ 2

= 56.5 mµs

0.5 µs/cm 2v/cm Ground reference at center Measured with 545 oscilloscope

Figure 82

B. Minimum Pulse Width Required for "Read-in Control Pulse"

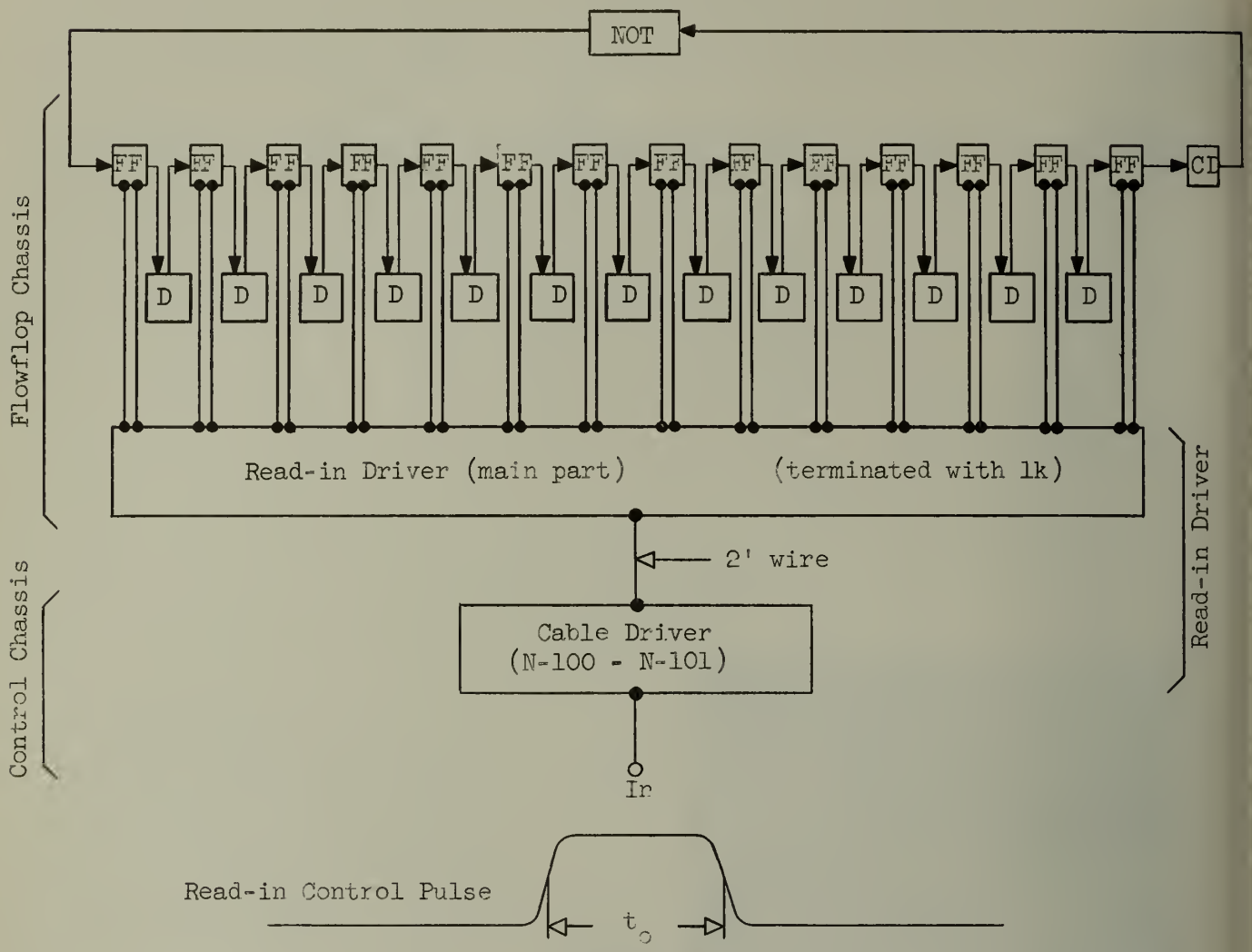


Figure 83

Since an artificial delay circuit is attached to each bit of the flowflop, the cycle time has no significance. The experiment was performed at 3mc pulse rate. The cycle time will be studied in Section C.

The schematic diagram of the "Read-in Control Pulse" generator is given by Figure 84.

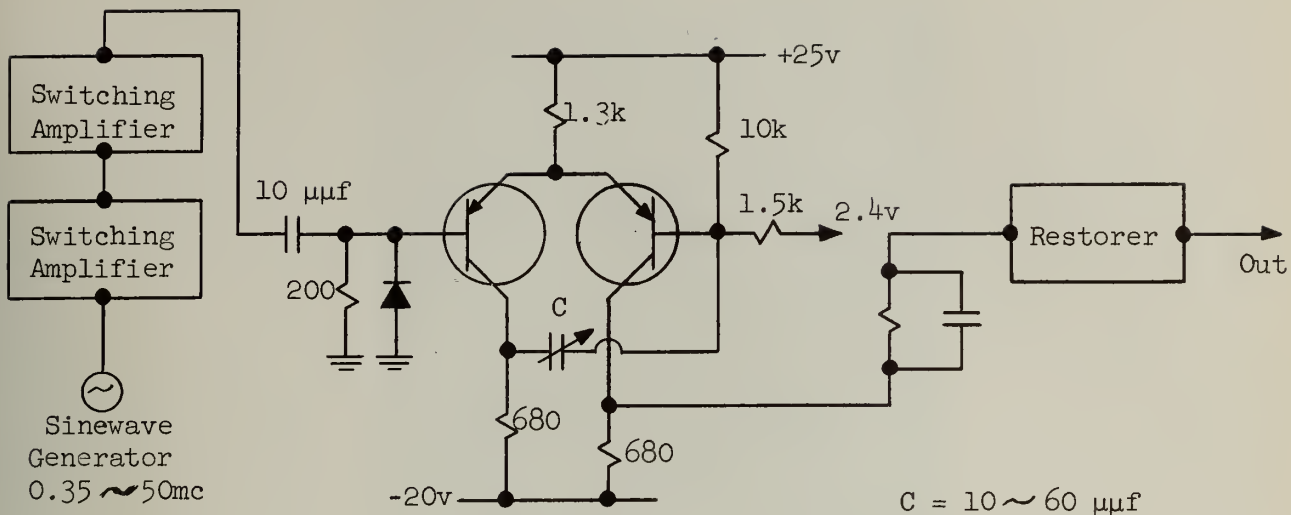
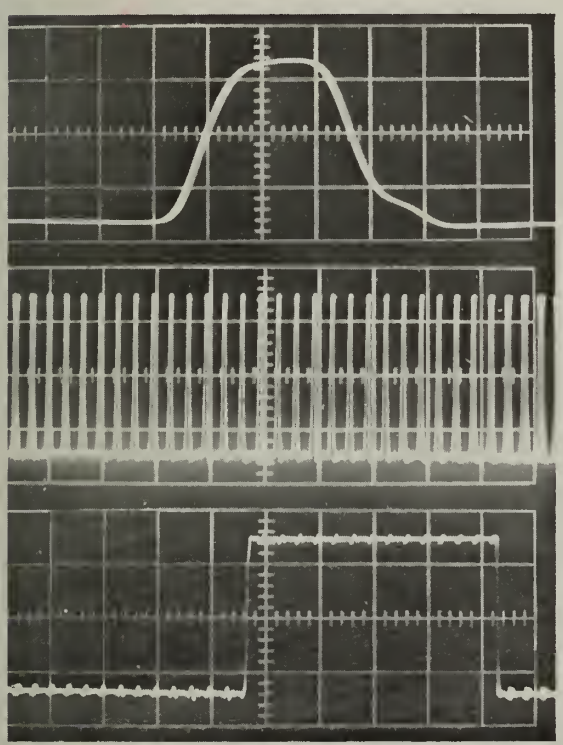


Figure 84



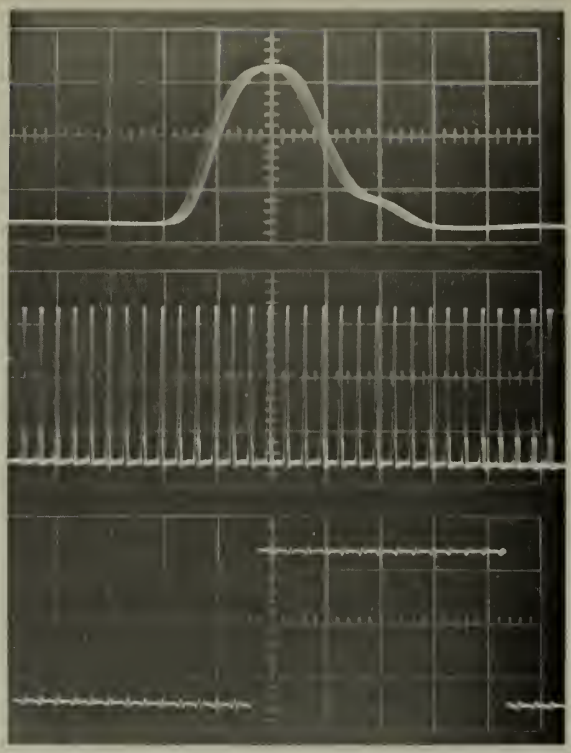
"Read-in Control Pulse"
2v/div., 20 mμs/div.

"Read-in Control Pulse" train
2v/div., 1 μs/div.

Input to the first bit position
2v/div., 1 μs/div.

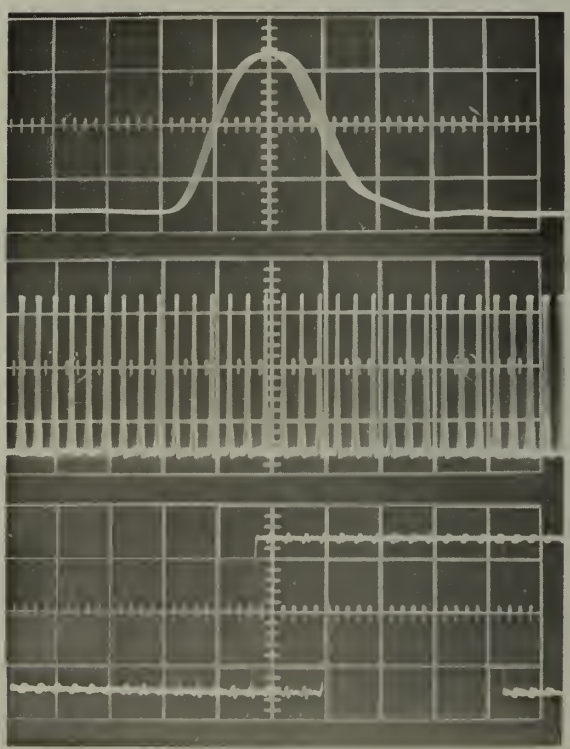
Perfect Operation

Figure 85



Critical
Operation

Figure 86
(Refer Figure 85)



Imperfect
Operation

Figure 87
(Refer Figure 85)

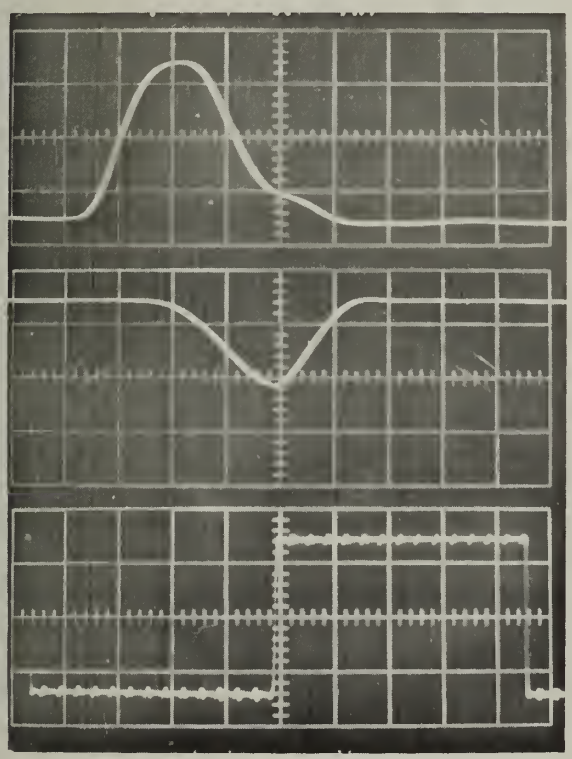
The minimum pulse width is subject to 1) the length of the wire connecting the flowflop chassis to the control circuit chassis, 2) the waveform of the "Read-in Control Pulse", and 3) the tolerance deviation of the flopflop register (including its driver), such as the variation of power supplies, the aging drift of resistors and transistors, etc. It will not depend on the cycle time. Among these three factors, the first two are terminal conditions. The third factor will be examined by the so-called marginal test.

C. Marginal Test

The test conditions are:

Nominal - ,	+25v,	+6.8v,	-5.0v,	-13.5v,	-50v,
6% up	+26.5v,	+7.3v,	-4.7v,	-12.0v,	-47v,
6% down	+23.5v,	+6.3v,	-5.3v,	-15.0v,	-53v,

Results are shown by the following pictures.

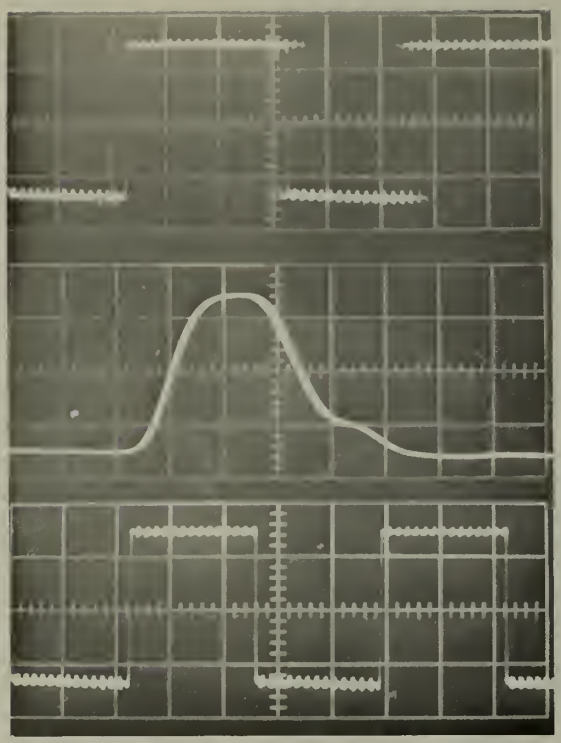


a) Minimum Read-in Control Pulse
All power supplies ± 0%
2v/div., 20 mμs/div.
This is by definition the nominal pulse.

b) R-2 Driver Output
5v/div., 20 mμsec

c) Register (input to the first bit)
2v/div., 1 μsec/div.

Figure 88



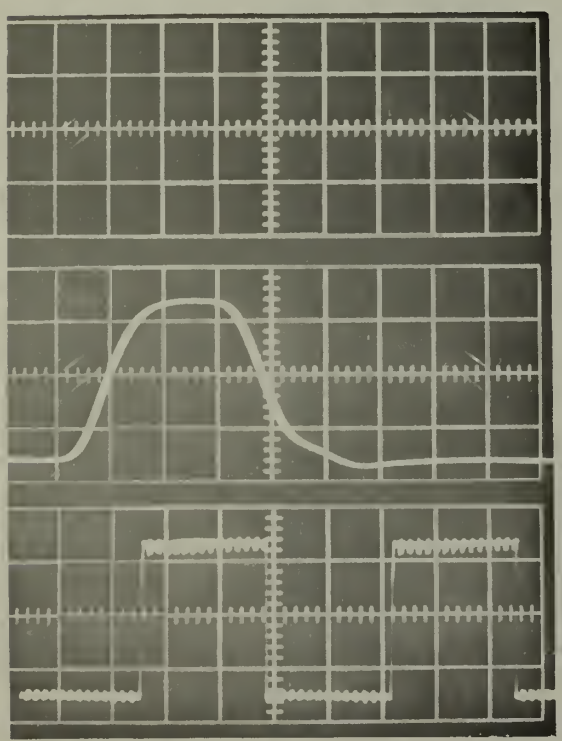
All power supplies +6%

a) Response to the Nominal Pulse
Operation is incomplete.
2v/div., 2 μsec/div.

b) The Minimum Pulse for Perfect Operation at +6% Deviation
2v/div., 20 mμsec/div.

c) Register (input to first bit)
2v/div., 2 μsec/div.

Figure 89



All power supplies -6%

a) Response to the "nominal pulse"

b) The Minimum Pulse for Perfect Operation at -6%
2v/div., 20 mμsec/div.

c) Register (input to first bit)
2v/div., 2 μsec/div.

Figure 90

The results are summarized in Figure 91. From these results, the following conclusions may be drawn.

1) The flowflop is optimized dynamically as well as statically, because it shows the shortest minimum pulse width at the nominal conditions.

2) The safety factor of 2, i.e., 88 mμs pulse width, will be sufficient in a practical case.

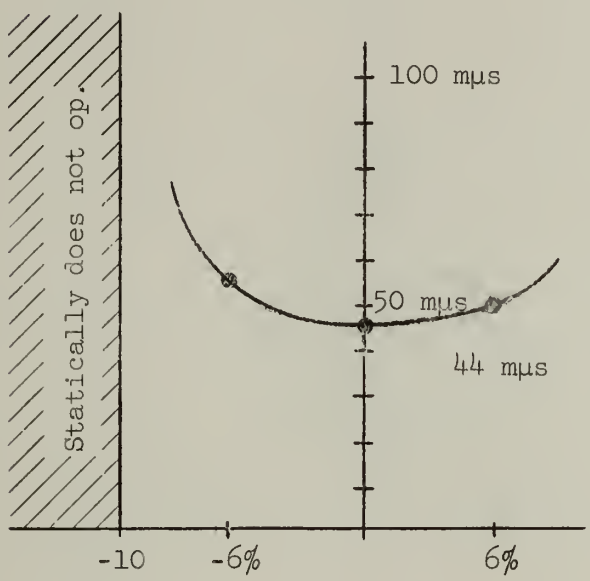


Figure 91

D. Cycle Time

The cycle time was tested by the scheme shown in Figure 92. In order to obtain the minimum cycle time all outputs of 14 flowflops were left independent. The attempted direct measurement of the minimum cycle time was unsuccessful because the switching speed of flowflops with their output terminals isolated was so fast that the monostable pulse generator could not generate the desirable patterns at high frequencies (higher than 10 mc). The switching time required of the flowflop by the systems group is 150 mμs. Therefore, if the registers operate at a 7 mc rate this requirement may be said to be satisfied. The basic flowflop register ("basic" means the tested flowflop's output is independent) operated at 7 mc without any difficulty.

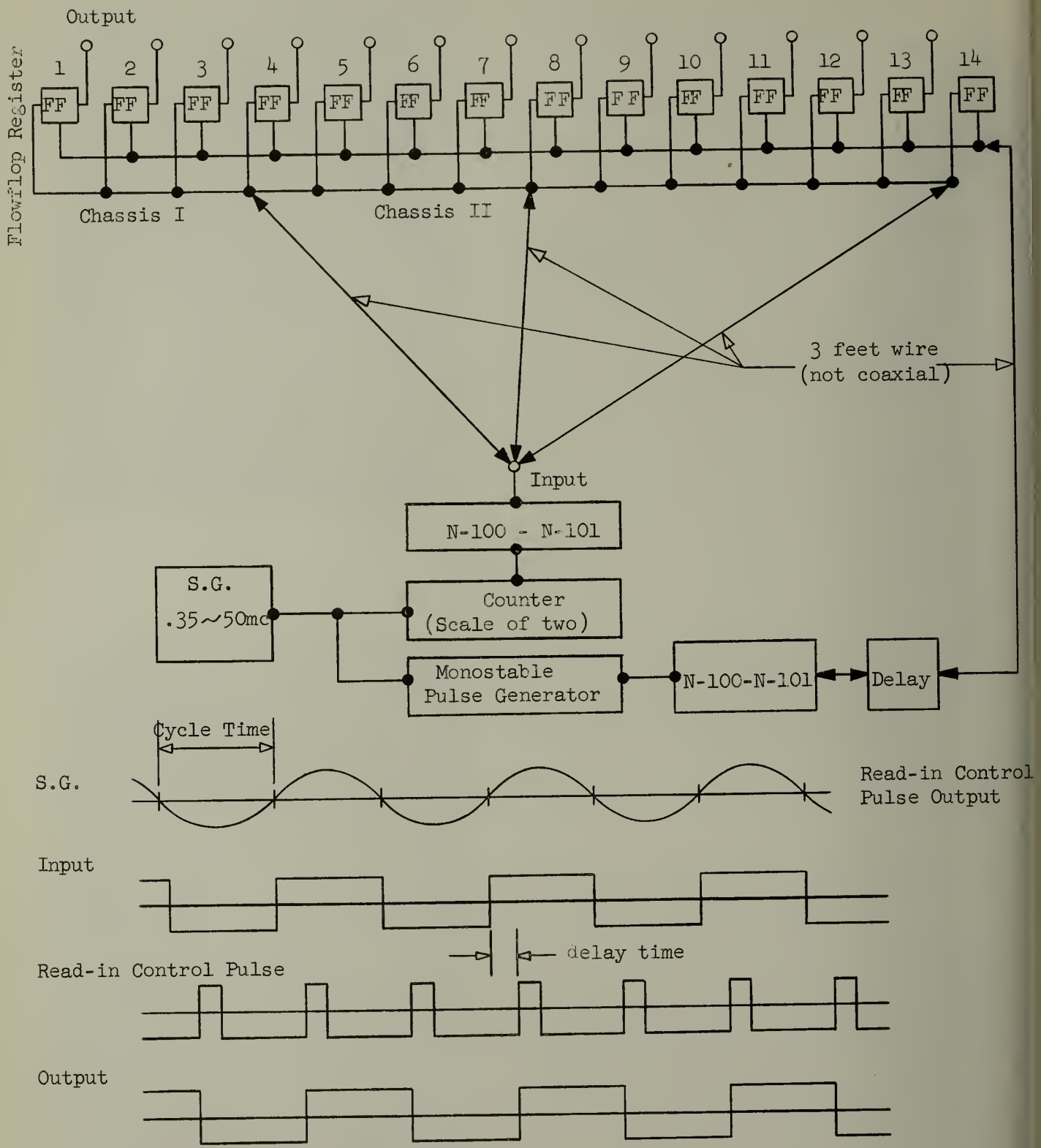


Figure 92

Schematic Diagram of Testing Circuits and
Expected Waveforms Neglecting all Transient Times

The indirect estimation of cycle time will be performed by measuring the following transient times:

1) Minimum "Read-in Control Pulse" Width t_w

2) Read-in Driver Transient Time t_1, t_2

3) Gate-in Time t_3

4) Gate-in Transient Time t_4

These are defined by Figure 93.

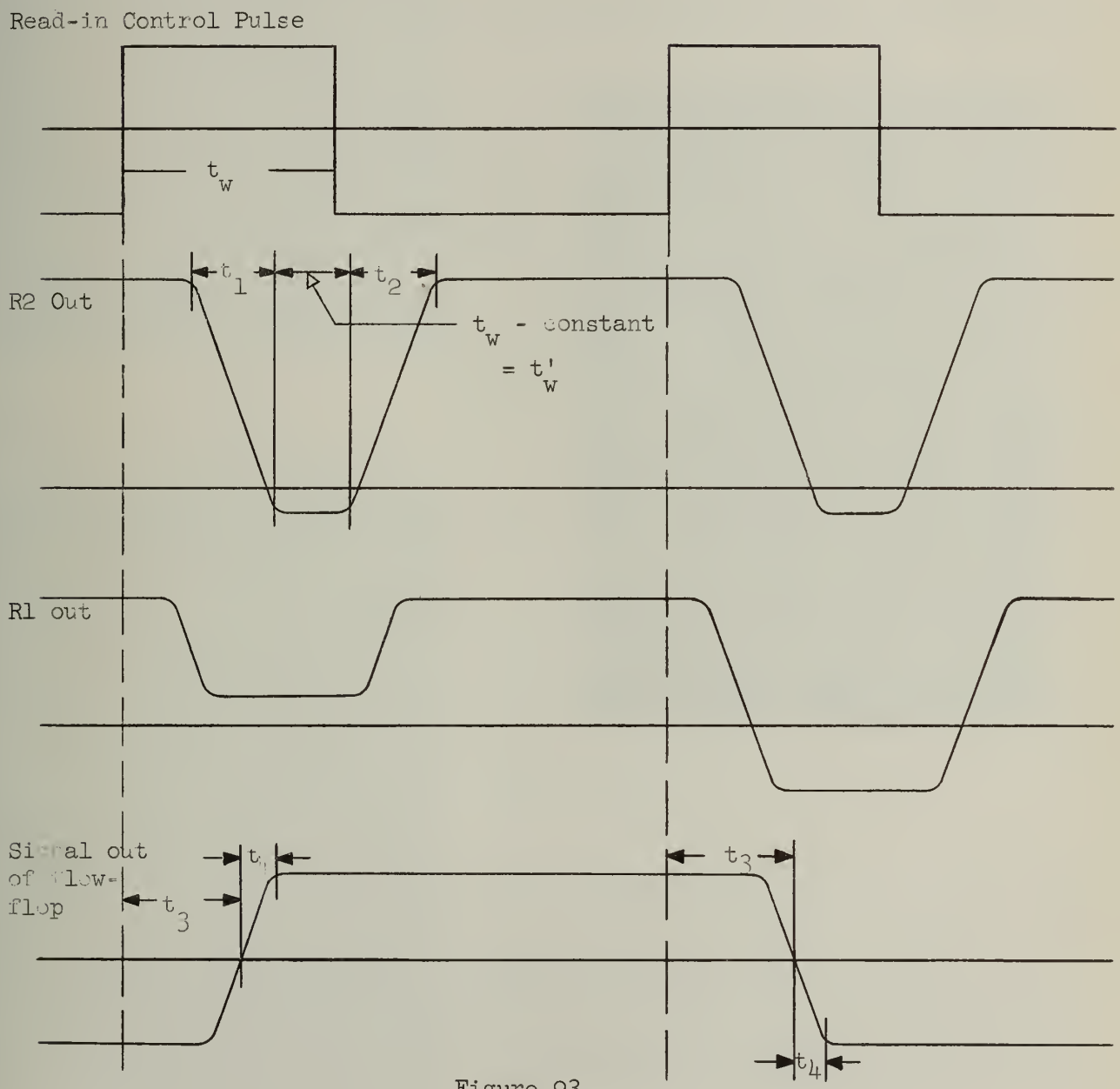


Figure 93

The minimum cycle time is the larger of

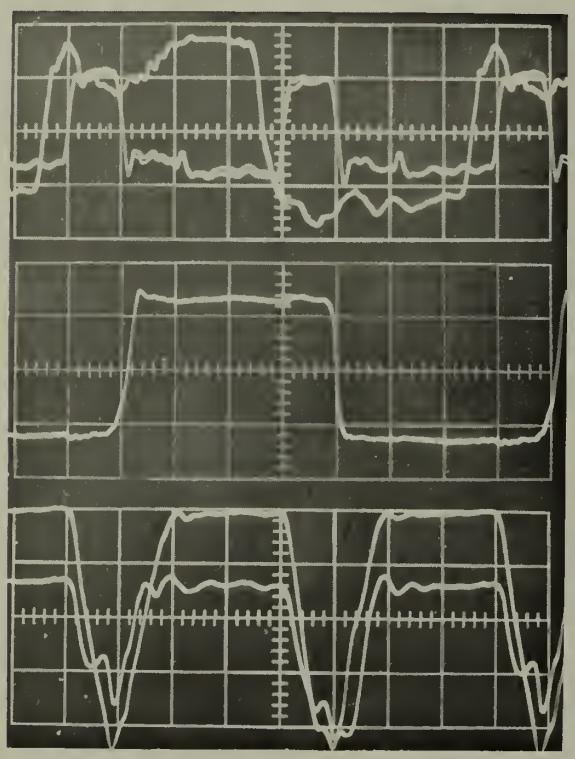
$$t_1 + t_2 + t'_w \quad \text{and} \quad t_3 + t_4 \quad .$$

If $$t_1 + t_2 + t'_w > t_2 + t_4 \ ,$$

the cycle time is driver-limited. If

$$t_1 + t_2 + t'_w < t_3 + t_4$$

it is flowflop-limited. Measured waveforms are shown in the following pictures.



Signal Input to the Flowflop

Ground

Read-in Control Pulse with Delay
50mμsec/div., 2v/cm

Ground

Signal output
50 mμsec/div., 2v/div.

R2 output

R1 output

Ground for R1

50 mμsec/div., 2v/div.

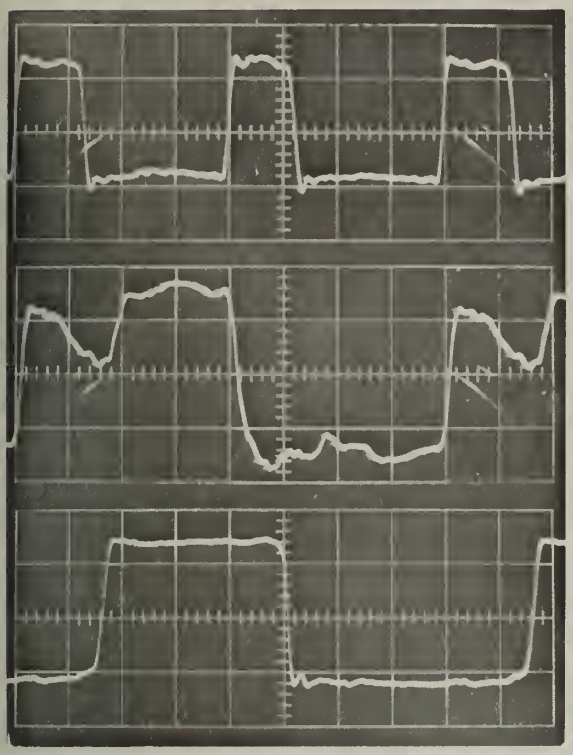
Ground for R2

Figure 94

The ripples are due to the connecting wires.

Since the outputs R1 and R2 are delayed by 20 or 30 mμs after the Read-in Control Pulse occurred, the simultaneous application of both the signal and the Read-in Control Pulse is perfectly permissible unless the waveforms of the input signal are too slow.

The waveforms of the simultaneous operation are shown in Figure 95.



Read-in Control Pulse

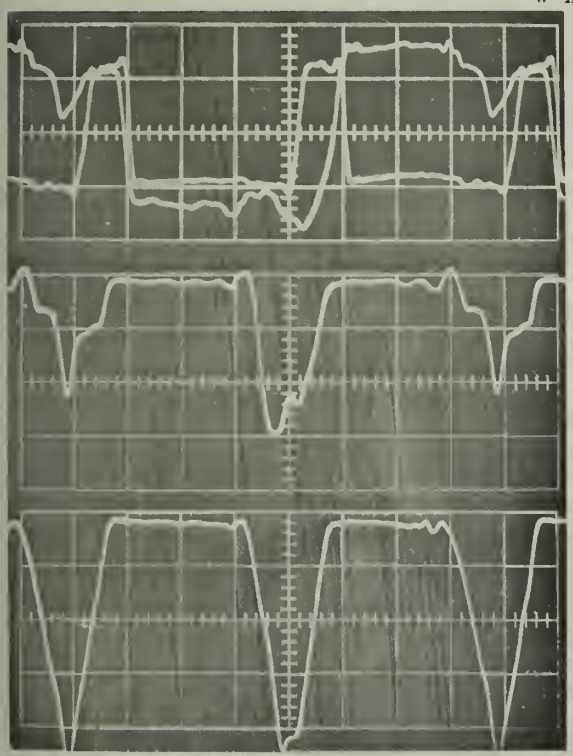
Input Signal

Signal Output

50 mμs/div., 2v/div.

Figure 95

Minimum pulse width operation $(t_w)_{min}$ is shown in Figure 96.



Signal Input

Read-in Control Pulse

R1

R2

2v/div., 50 mμs/div.

Figure 96

From these pictures we may conclude:

(1) $(t'_w)_{min} = 0.$

(2) The case is driver-limited.

At normal conditions,

$$(t_1 + t_2)_{min} \cong 100 \text{ m}\mu\text{s}$$

$$t_w = A5 \sim 55 \text{ m}\mu\text{s}$$

$$t'_w = 0$$

$$t_s = 50 \sim 65 \text{ m}\mu\text{s}$$

$$t_4 = 10 \sim 15$$

Conclusion:

Unless the output circuits (11-AND) increase the t_3 and t_4, the cycle time is driver-limited and at a maximum of 10 mc.

E. Read-Out Test

The read-out tests concern themselves with the following circuitry:

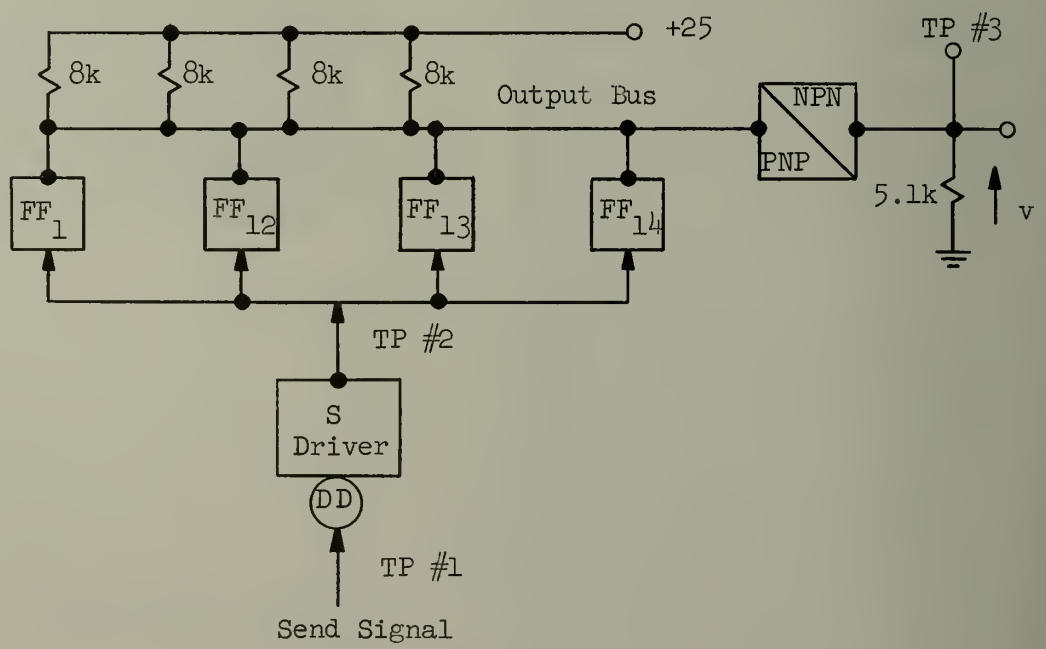


Figure 97

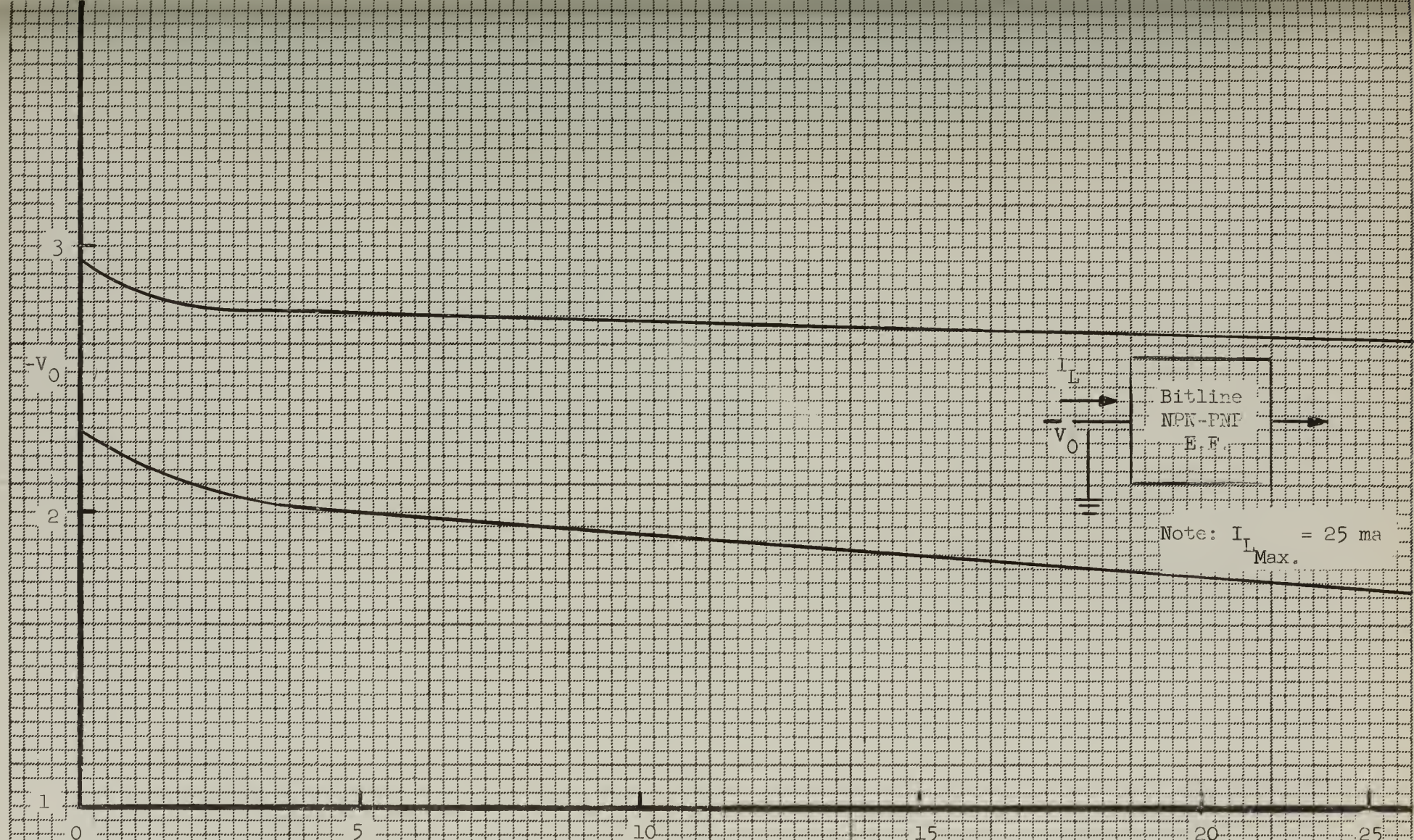


Figure 98

Loading Effect (Static) Flow-Gating

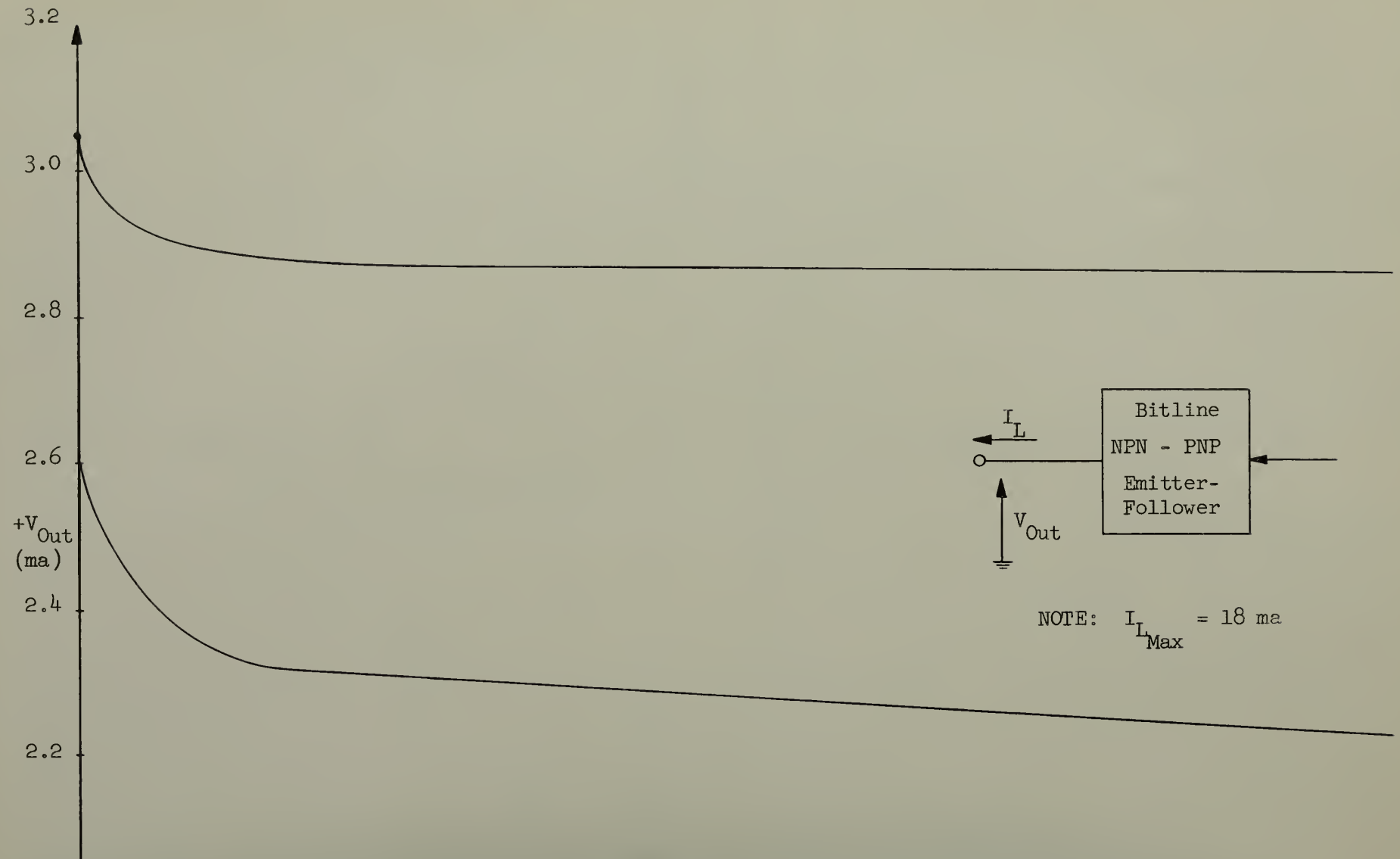


Figure 99

Load Effect (Static) Flow-Gains

a) DC-behavior

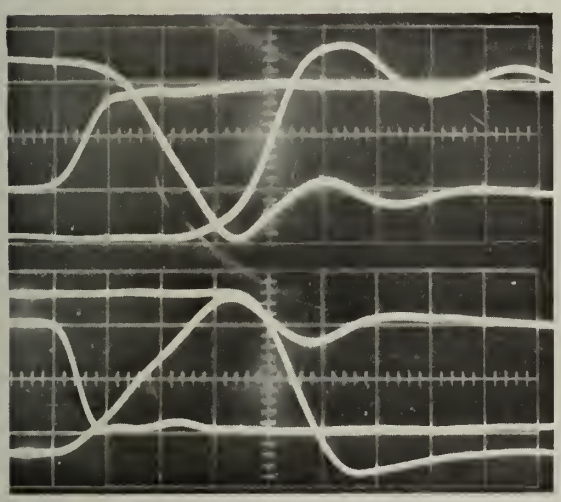
The loading effects are shown by the two static loading curves. The output impedance is clearly less than 160 ohms.

b) Dynamic Behavior

Test I: In order to study the delays in the circuit, a relay-pulse test was performed by the following method:

1. Set all fourteen flipflops to zero. This constitutes maximum load for the driver.
2. Disconnect all flipflops from output bus except the one furthest removed from the termination emitter-follower.
3. Load the output bus with 180 ohms in parallel with 5.1k resistor.

The results of the test are shown in Figure 100.



a) Reset edge of Send Circuit
TP #3, TP #1, TP #2
(top to bottom)

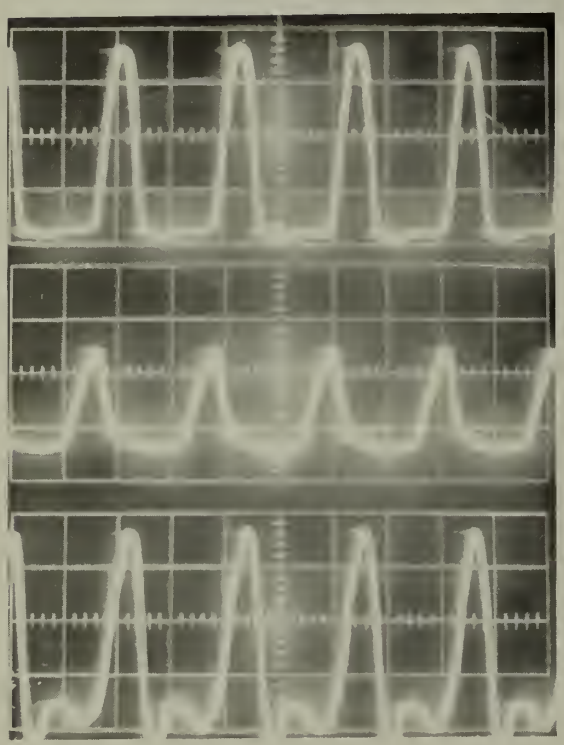
b) Send:
Scale: 1.4v/cm, 10 nsec/cm
TP #2, TP #1, TP #3
(top to bottom)

Figure 100

Hence, the experimental operation time appears to be 40 nsec to send and 35 nsec to reset. It is believed that a safety factor of two will account for tolerance drifts and load changes, so that it is believed that the read-out time is not more than 80 nsec in either direction.

Test II (Interconnection Behavior): The testing procedure is the same as in Test I except that the delay pulser is replaced by a pulse generator. The test points are:

a) TP #1 - Input send signal
b) TP #2 - Output bus
c) TP #3 - Output of flipflop without bus



All scales: 2v/cm
50 nsec/cm

TP #3, TP #1, TP #2 (Top to Bottom)

Figure 101

V. PHYSICAL LAYOUT

Considerable efforts were made to obtain a layout which is favorable as far as electrical characteristics and physical compatability with the interconnecting systems are concerned. The two categories do, of course, conflict with one another (Murphy's Law).

As far as electrical characteristics are concerned, two points are to be considered: a) instability due to wiring effects, b) speed losses due to wiring.

The stability problem cannot be solved uniquely by layout only. For this reason circuit design should concern itself with this point. Insertion of unconditionally stable circuitry in doubtful cases is not only desirable but necessary. The conclusion is that DC-design without AC-consideration is insufficient. However, careful layout considerations tend to minimize the use of stabilizers. The precautions to be taken are:

1. Base leads in emitter-followers must be short. Instability occurs if the equipment base inductance is 0.2 microhenries or less, depending on capacitive load. The use of complementary emitter-followers does not eliminate instability, but it does reduce it.

2. If an emitter-follower is driven in such a way that diode circuitry is connected to its base, the diodes should be connected to the base of the emitter-follower and not any other place.

3. Decoupling networks, if used to stabilize bumping supplies, must be connected directly to the signal driver, and, if the stabistor supply has several signal diodes connected to it, each one must be bypassed.

The problem of speed losses due to wiring is probably worse than that of stability. It was found experimentally that signal busses of approximately 1 meter length will decrease the rise time of the signal by factors of up to three, if the input rise time is about 10 nsec. Experiments show that the degradation may be lessened by moving the signal wire away from the ground plane. The spacing becomes now critical somewhere between 0.5 and 1 cm spacing, and was found to be dependent on sending and receiving end impedances. Studies in this field are incomplete, but are being continued. It may be said, however, that for the system considered, the previously stated spacing is optimum. It should be pointed out that the method of

grounding the chassis plane itself is important. Here the rule of "the more the merrier" seems to apply. As pointed out earlier, the signal bus system presents in itself some peculiar problems. It was found that signal degradation is less if the bus impedance is distributed along the line. For example: the output circuit employs a single wire which is connected to each flipflop. The impedance level is about 2000 ohms. This resistor was distributed along the line in four parts of 8000 ohms each.

In summary form then: If rise times of 10 nsec are to be maintained the bandpass of the circuitry is 35 MCS. At this frequency layout is as important as basic design and should be considered a part of it. Therefore, eye-pleasing construction techniques should be sacrificed for functional behavior. The study of transistors and suitable high-speed topology in itself is insufficient if not accompanied by a similar study of interconnecting techniques.

The system which is being considered is proposed to have 11 words. The words are arranged in 1/4-word units as shown in Figure 102. Each word uses two rows of transistors. The row between two words is used for driver location. Input and output signals are located on vertical busses, driver signals on horizontal ones. The bit distribution of 4:4:6 is forced by minimum skewing to input and output equipment. A unit of this type containing 2 1/4 words has been built along these lines and is currently undergoing tests by the systems group. There were no important difficulties in respect to performance. The final unit is under construction.

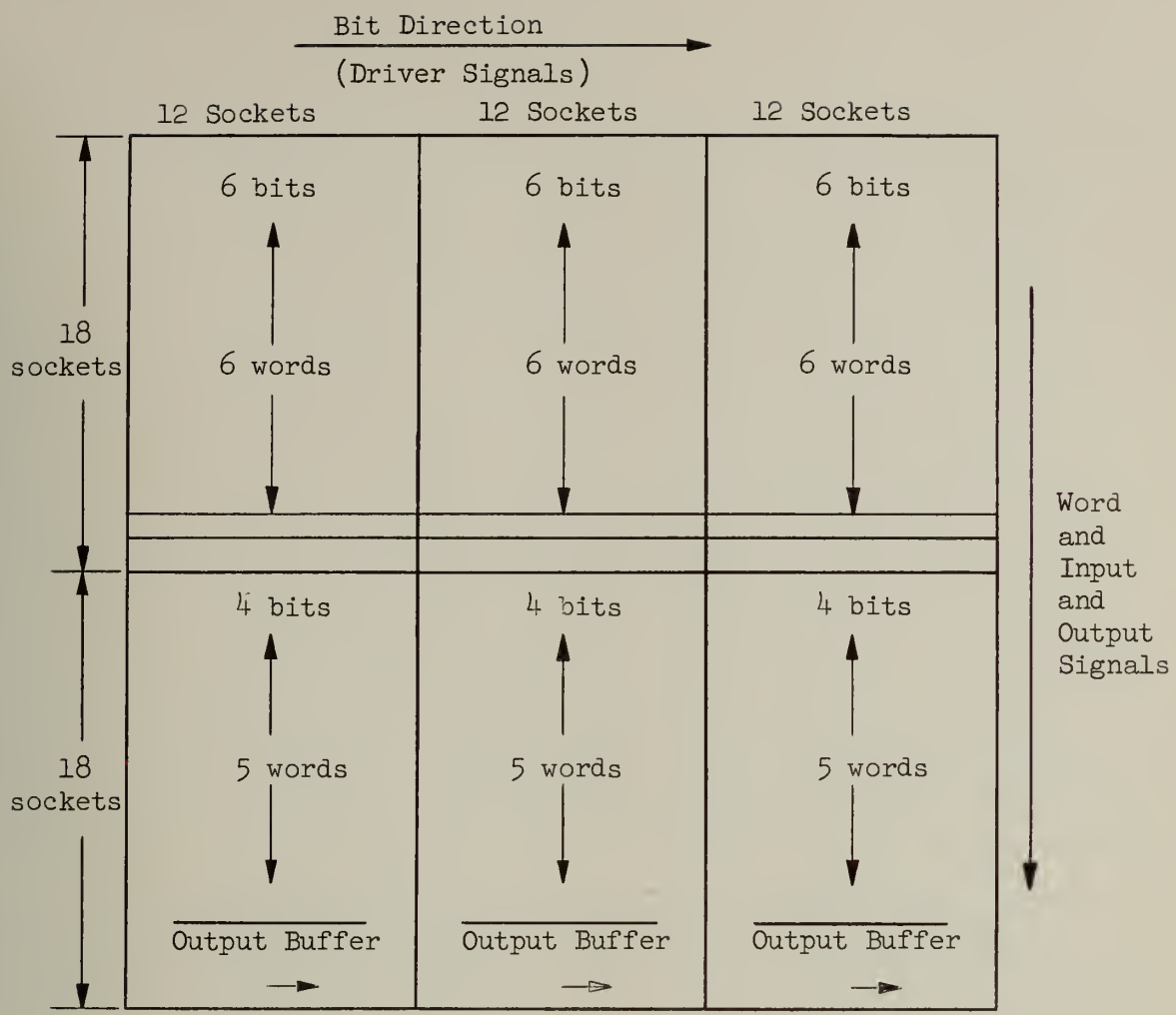

Bit Direction
(Driver Signals)
12 Sockets
12 Sockets
12 Sockets
6 bits
6 bits
6 bits
18 sockets
6 words
6 words
6 words
Word and Input and Output Signals
4 bits
4 bits
4 bits
18 sockets
5 words
5 words
5 words
Output Buffer
Output Buffer
Output Buffer

Figure 102